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1.06 MICRON HIGH SENSITIVITY IR PHOTOCATHODE.(U)
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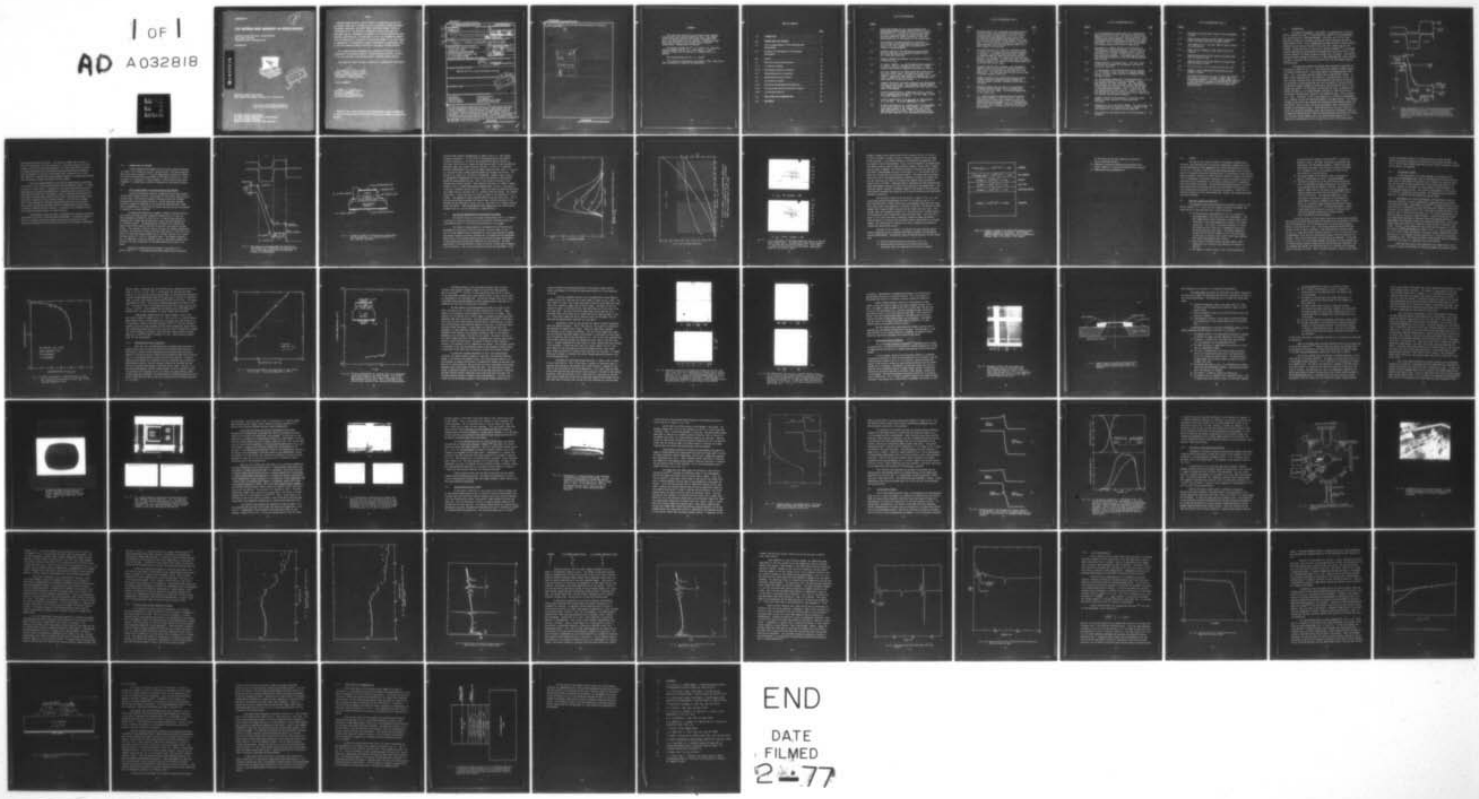

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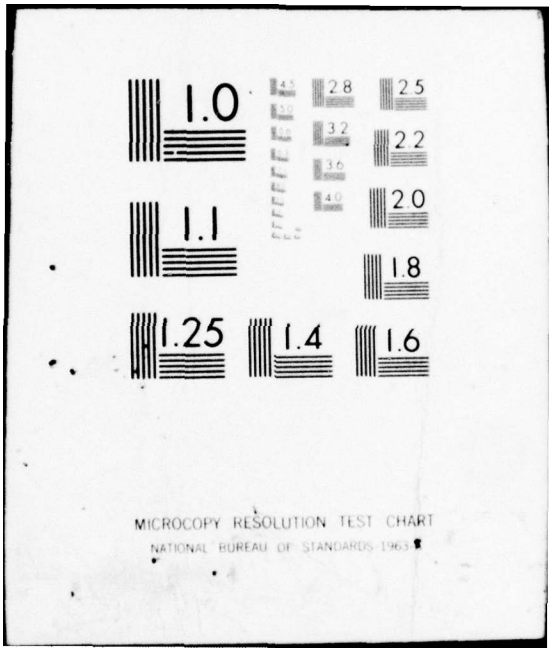
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# 1.06 MICRON HIGH SENSITIVITY IR PHOTOCATHODE

*SCIENCE CENTER, ROCKWELL INTERNATIONAL*
*1049 CAMINO DOS RIOS*
*THOUSAND OAKS, CALIFORNIA 91360*

OCTOBER 1976






TECHNICAL REPORT AFAL-TR-76-94
FINAL REPORT FOR PERIOD 6 JANUARY 1975 - 30 JUNE 1975



AIR FORCE AVIONICS LABORATORY
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The design and progress toward realization of a high sensitivity 1.06μm field-assisted heterojunction photocathode are reported. Major emphasis has been placed on developing a Cs activation process for heterojunction devices and on a device fabrication technology which is consistent with Cs activation requirements. The first heterojunction devices (cold cathodes) were successfully activated and emission into vacuum was observed. Further work in developing a heterojunction photocathode structure for activation is recommended in order →

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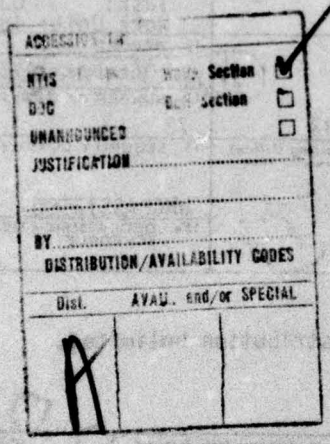
to realize the complete device and demonstate the potential of the hetero-junction photocathode.



## FOREWORD

This report was prepared by the Science Center, Rockwell International under contract F33615-75-C-1037. This report covers the period 6 January 1975 through 30 September 1975 and is the Final Report on this contract. The work described herein was carried out by the Science Center, Rockwell International, Thousand Oaks, California.

The project engineer was Dr. J. S. Harris, Jr. Associate project engineers were Dr. R. C. Eden and Dr. R. Sahai. Technical support was provided by L. O. Bubulac and J. R. Waldrop.

The program manager was Dr. A. S. Joseph

This report was submitted by the authors in May, 1976 and has been reviewed and is approved for publication.

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## 1.0 INTRODUCTION

The research discussed in this report is a continuation of previous efforts (#F33615-72-C-1921[1,2] and #F33615-74-C-1085[3]) for the development of a high sensitivity 1.06μm photocathode. The design goal for this high sensitivity cathode is an external quantum efficiency (electrons emitted/incident photon) of 20%. Such a photocathode has been pursued at several research laboratories over the past few years but as yet such a device has not been realized. During the course of the earlier research programs[1-3], we designed a double heterojunction photocathode and demonstrated the feasibility of field-assisted transport of thermal electrons through such a structure. The measured internal electron transport efficiency at 1.06μm approached 70%, clearly showing that with a reasonable NEA surface one should reach the 20% external quantum efficiency goal.

An energy band diagram illustrating the principles of operation for this device is shown in Fig. 1.1. This energy band diagram is drawn assuming no "abrupt discontinuities" in the energy bands at the heterojunction interfaces. Fig. 1.1(a) shows the energy bands with no applied bias voltage. It shows a large "potential well" for electrons in the hole barrier region. As bias voltage is applied across the emitter-absorber (the polarity is positive to the emitter so that the absorber-hole barrier junction is reverse biased), the depletion region increases in width across the hole barrier until it just reaches the emitter. At this point, the hole barrier layer is completely depleted (identical to the "punch-through" condition in a PNP transistor) and no electron "potential well" remains in the conduction band. This is shown in Fig. 1.1(b). The device in Fig. 1.1(b) operates as a reflective photocathode (i.e., photons incident and electrons emitted at the same surface). The photons incident on the device pass through the transparent (wide bandgap) emitter and hole-barrier layers to reach the narrow gap absorber where a photoelectron is created in the conduction band. These photoelectrons now have a "down hill slide" (via drift and diffusion) across the hole barrier and emitter layers to the Negative Electron Affinity (NEA) surface where they are emitted into vacuum. The hole bias current remains low on this device because there is still a significant (approximately 0.40 eV) potential barrier in the valence band at

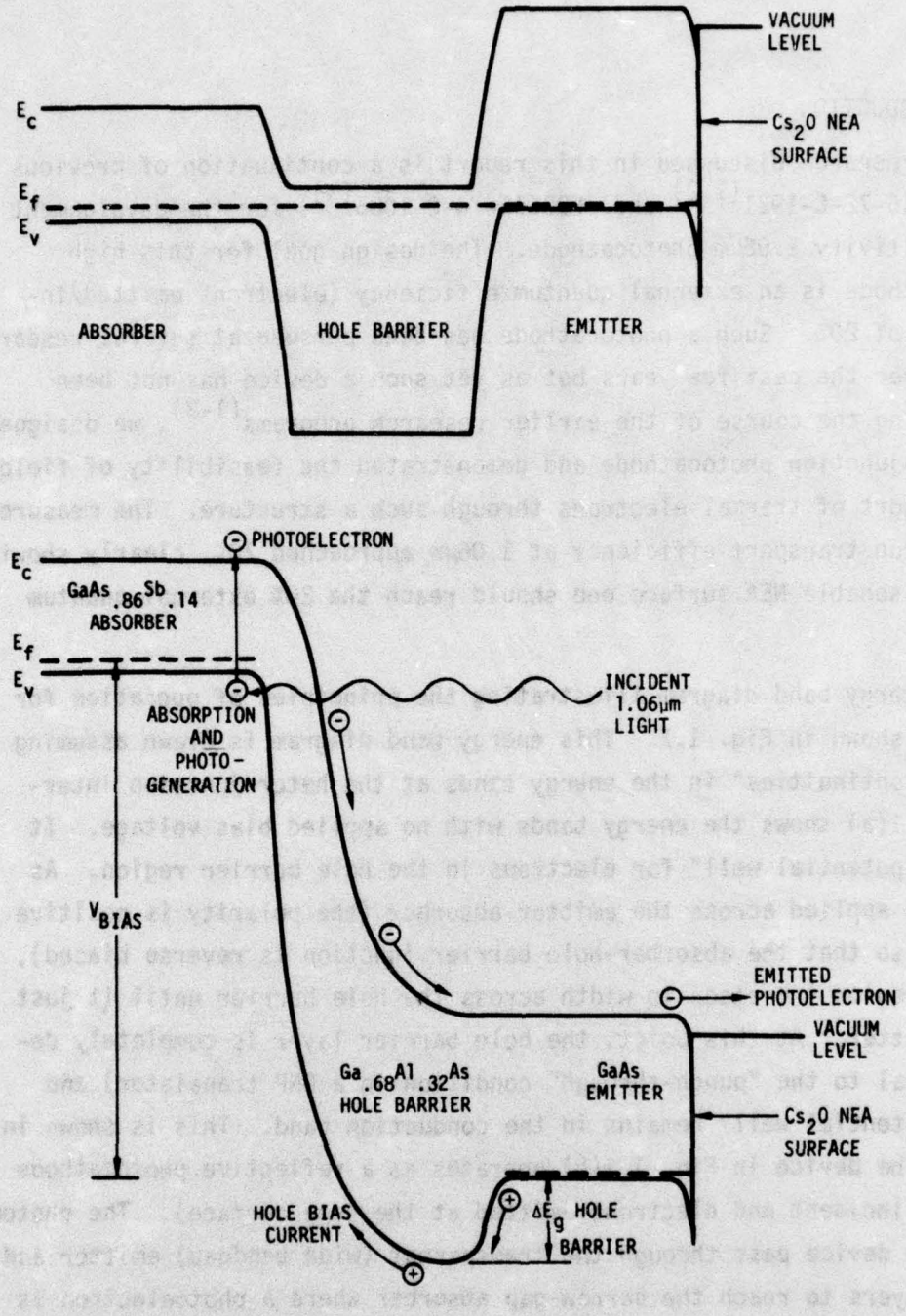



Fig. 1.1 Energy band diagram for the 1.06μm heterojunction photocathode assuming graded junctions with no "abrupt discontinuities." (a) the p-n-p device at zero bias. (b) The p-n-p device biased to "punch through" under operating conditions showing no barrier in the conduction band and ~ 0.4 eV barrier in the valence band.

the emitter-hole barrier junction. This barrier prevents the injection of holes from the emitter into the hole barrier. The proper selection of bias voltage, doping level and energy bandgap of all three layers make it possible to achieve the monitonically decreasing conduction band profile proceeding from the absorber all the way to the vacuum level as shown in Fig. 1.1(b). This condition is necessary for the unimpeded transport of thermalized electrons from the absorber through the emitter and into vacuum.

Our prior accomplishments on this device unquestionably established the validity of the above double heterojunction photocathode concept. In order to realize a useful device, a compatible Cs activation and device processing technology were pursued for production of a suitable emitter surface on the heterojunction device for Cs activation. Device structures were successfully fabricated (including ohmic contacts) which could withstand the thermal treatment (610°C) required in the activation process. A Cs activation chamber specifically designed for field-assisted photocathodes was built and both passive GaAs surfaces and the GaAs surfaces of heterojunction devices were activated to negative electron affinity. In addition, cold cathode emission into vacuum was observed from a p-n heterojunction.

Considerable progress was made in developing the necessary processing technologies to realize a field-assisted photocathode. A continuing research effort is, however, required to improve the device structure and surface passivation techniques so that this device can reach its potential performance.

## 2.0 PROGRAM GOALS AND APPROACH

A high performance photocathode with 20% external quantum efficiency at 1.06μm is the ultimate goal of this research program. The major accomplishment of our earlier programs [1-3] was the demonstration of the basic concepts of the double heterojunction photocathode as described in Section 1.0. Since this work is a continuation of those programs, a brief review of these accomplishments is included here to provide a background for the present investigation.

### 2.1 Prior Accomplishments on the Heterojunction Photocathode

The major technological problems in demonstrating the double heterojunction device concept involved 1) the growth of a multi-layer, heterojunction structure and, 2) the electron transport properties of both the individual heterojunctions and the complete structure. Because these basic problems centered on growth and properties of the appropriate heterojunctions, rather than on photoemission, a simpler device structure was used to avoid the problems of preparing Cs activated surfaces.

An energy band diagram and a schematic drawing of the test structure best suited to solving the above problems are shown in Figs. 2.1 and 2.2. The band diagram is identical to that of Fig. 1.1 (both at zero bias and at operating bias), except that the NEA emitter surface has been replaced by a p-n junction collector. The photoelectrons collected at this junction are those electrons which would be available for emission into vacuum at the NEA surface. This collector current is used to calculate the internal photoemission efficiency, and the overall external efficiency would just be P times this value, where P is the surface escape probability for a thermal electron at a Cs activated GaAs surface ($P \sim 0.25$ is a reasonable value). The schematic diagram in Fig. 2.2 shows the p-n junction collector structure, the nominal chemical compositions, the layer thicknesses, and the doping densities for each of the layers.

Devices of the above type were processed as described in our earlier reports[1-3]. A photoresponse measurement demonstrating the measured

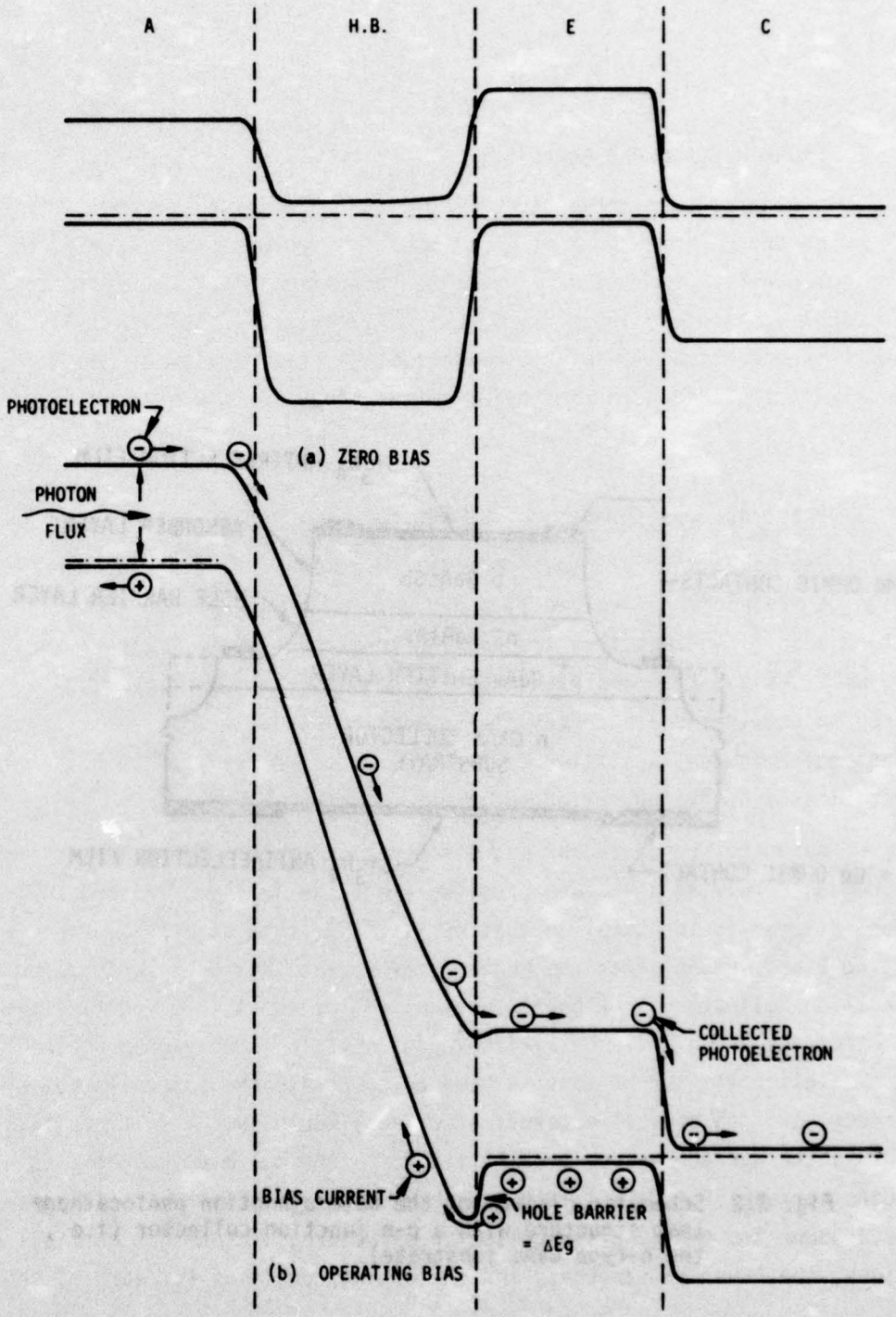



Fig. 2.1 Band diagram of the photocathode test structure at (a) zero bias and (b) operating bias where the n-type layer at the right replaces the Cs activated NEA surface of the photocathode.

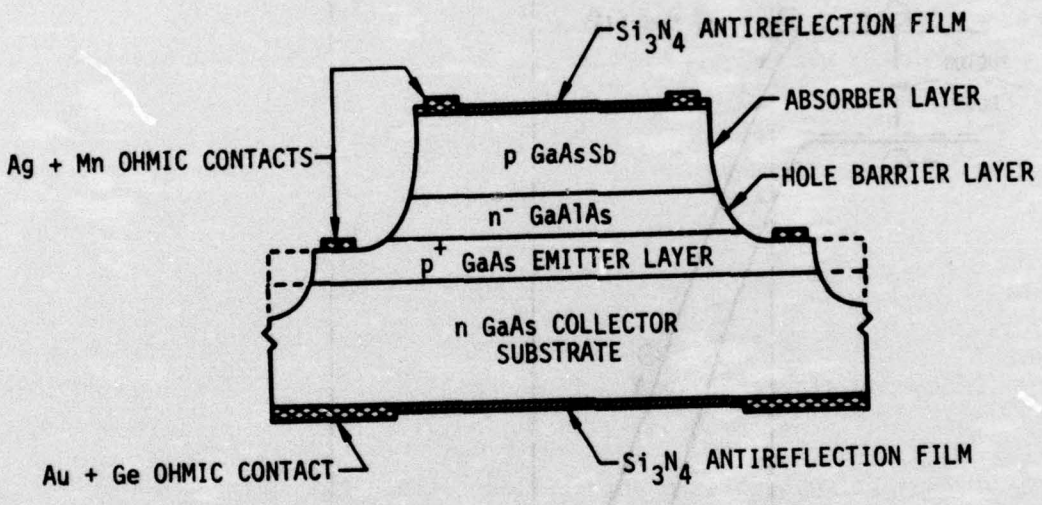



Fig. 2.2 Schematic diagram of the heterojunction photocathode test structure with a p-n junction collector (i.e., the n-type GaAs substrate).

field-assisted internal photoemission is shown in Fig. 2.3. The internal transport efficiency, $\alpha$, is the ratio of the photocurrent at the emitter-collector junction, $I_c$, to that at the absorber-hole barrier junction $I_a$. The actual total value of $I_c$ cannot be used because there is some photocurrent generated within the emitter-collector junction. In Fig. 2.4 a corrected collector photocurrent, $\Delta I_c$ and $I_a$ are shown along with their ratio ($\alpha = \Delta I_c / I_a$) as a function of bias voltage applied between the absorber and emitter. The values of $\Delta I_c$ and $I_a$ are a function of wavelength. However, their ratio, $\alpha$, is independent of wavelength and high transfer efficiency is observed even though the photocurrents are low. This is due to poor collection at the absorber-hole barrier junction. Good transfer efficiency at 1.064$\mu$m is demonstrated in Fig. 2.5 where the measured photocurrents, $I_a$ and $I_c$, are shown as a function of position across a device. These line scans are obtained utilizing the 1.064$\mu$m line of a Nd:YAG laser in a scanning light microscope. The transfer coefficient $\alpha$ is just the ratio of $I_c$ and $I_a$ (there is no correction in $I_c$ at 1.06$\mu$m). The response is quite high and uniform along the entire scan. All of the non-uniformities along the line scan are due to surface features on the absorber and are reflected in both $I_a$ and $I_c$, thus their ratio remains constant across the device. These measurements clearly demonstrate that both high and uniform values of $\alpha$ can be obtained for 1.06$\mu$m operation.

## 2.2 Approach for Heterojunction Photocathode Development

The specific thrust of the present photocathode effort is to develop a full device structure and processing and activation techniques which will yield demonstration of a field-assisted photoemission into vacuum.

The change in program emphasis from demonstrating field-assisted photoemission with the p-n junction collector structure shown in Figs. 2.1 and 2.2 to the demonstration of photoemission into vacuum completely changes the program because an entirely different set of problems must be approached. Modification of the present heterojunction structure and major developments in the processing and activation technology will be required. The major modification in the new structure is that its emitter surface must be exposed for Cs activation. This is not a particularly difficult requirement if the

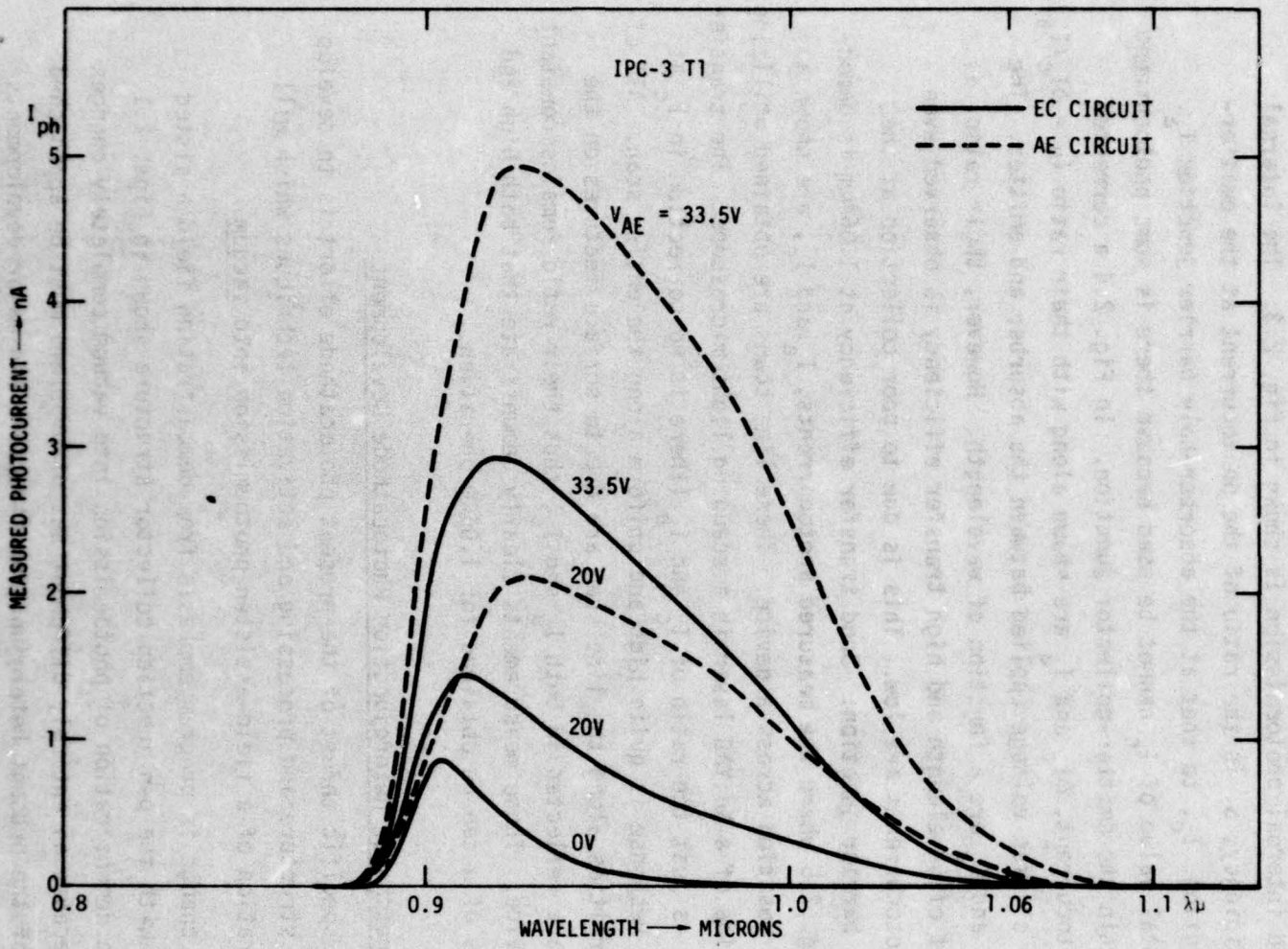



Fig. 2.3 Spectral response measurements in EC and AE circuits as a function of $V_{AE}$.

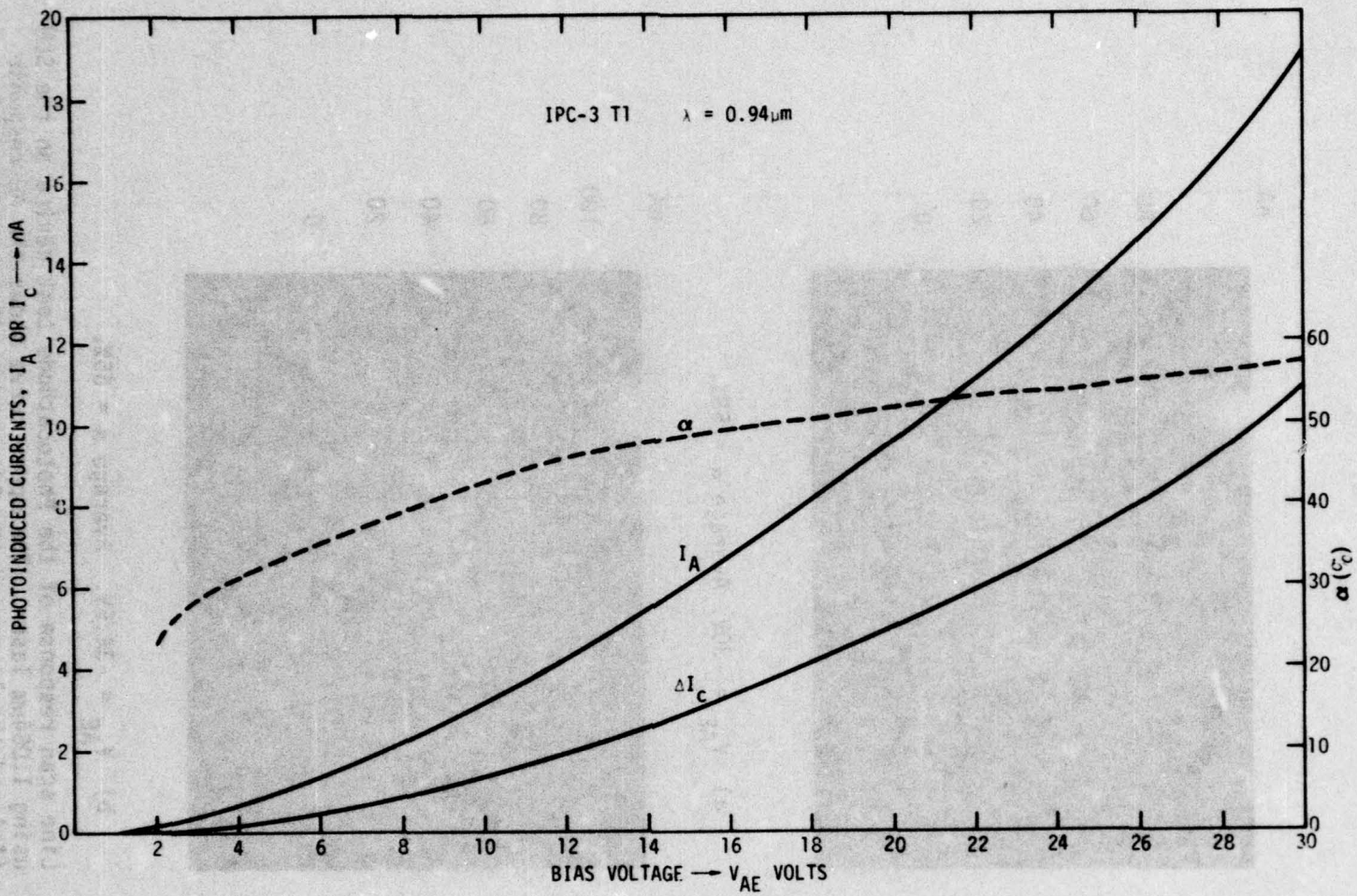
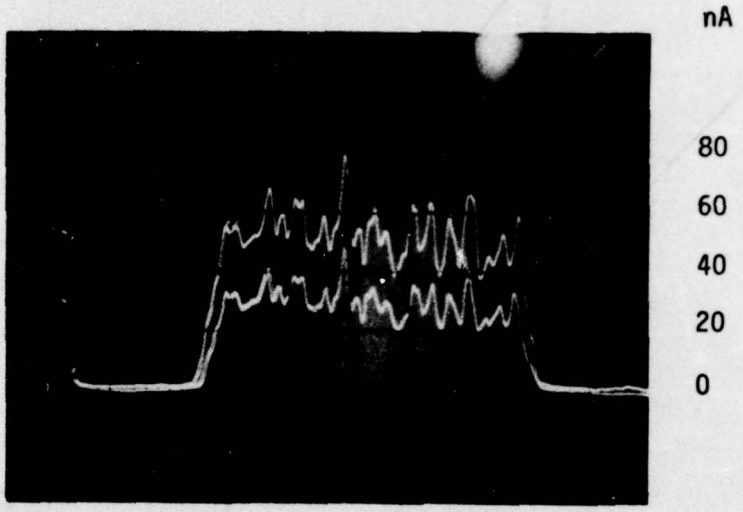
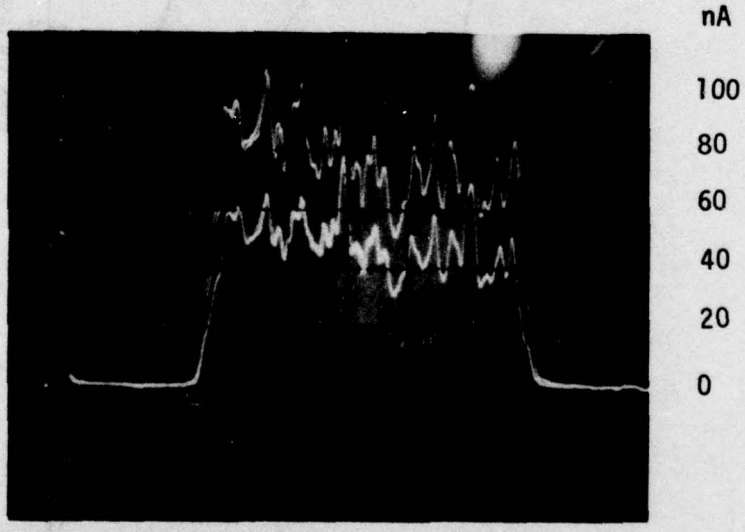



Fig. 2.4 AE circuit response - $I_A$, and the photocathode response in EC circuit - $\Delta I_C$ as a function of bias $V_{AE}$. α is the transfer coefficient as computed from $I_A$ and $\Delta I_C$ values.




a) $V_{AE}$ = -30V. Average $\alpha$ = 58%.




b) $V_{AE}$ = -34.5V. Average $\alpha$ = 65%.

Fig. 2.5 Line scan response of the Photocathode test device on the SLM using 1.064μm laser. The upper curve shows the AE response ($I_A$) and the lower one the EC response ($I_C$). Their ratio, $\alpha$, seems to be very uniform with the average value noted above for the two bias values.

cathode is grown in the reverse order to the structure in Figs. 2.1 and 2.2 so that the emitter is grown last and is naturally exposed as the top layer of the structure. This growth sequence is unfortunately an impossible task for growth by liquid phase epitaxy. In our earlier program[1], we demonstrated that GaAsSb could be grown on GaAs or GaAlAs, however, neither GaAs or GaAlAs could be grown on GaAsSb. This condition places a constraint on the direction with which a photocathode structure can be grown (i.e., the absorber must be grown over the hole barrier and emitter layers). This means that the emitter surface will be at the substrate-emitter interface at the end of growth, and that the substrate will have to be selectively removed before the emitter surface can be activated. Substrate removal techniques have been developed for other semiconductor devices and these can be applied to the photocathode. This substrate removal, however, introduces changes in the growth of the structure, significantly increases the complexity of the device processing and complicates the device evaluation.

The new device structure for activation is shown in Fig. 2.6. The active heterojunction photocathode structure is now grown on top of a $p^+$-GaAs substrate with a $p^+$-GaAs buffer and an intervening n-GaAs etch stop layer. The $p^+$-GaAs layer is Ge doped and is required to provide a Zn diffusion barrier between the Zn doped $p^+$-GaAs substrate and the n-GaAs etch stop layer. This $p^+$-GaAs layer just becomes an extension of the substrate and is etched away in the electrolytic etch to expose the n-GaAs etch stop layer. This etch stop layer is only 2-3$\mu$m thick and is chemically etched to expose the emitter. After processing, the device must be placed inside a high vacuum Cs activation chamber, the surface must be cleaned and Cs and $O_2$ sequentially applied to produce the required NEA surface.

The goal of this program is to develop the above heterostructure growth, processing and Cs activation techniques to produce a vacuum heterojunction photocathode. The specific tasks to realize this goal are the following:

1) Grow the new heterojunction structure of Fig. 2.6.
2) Develop bonding, processing and surface passivation techniques which are compatible with structural support

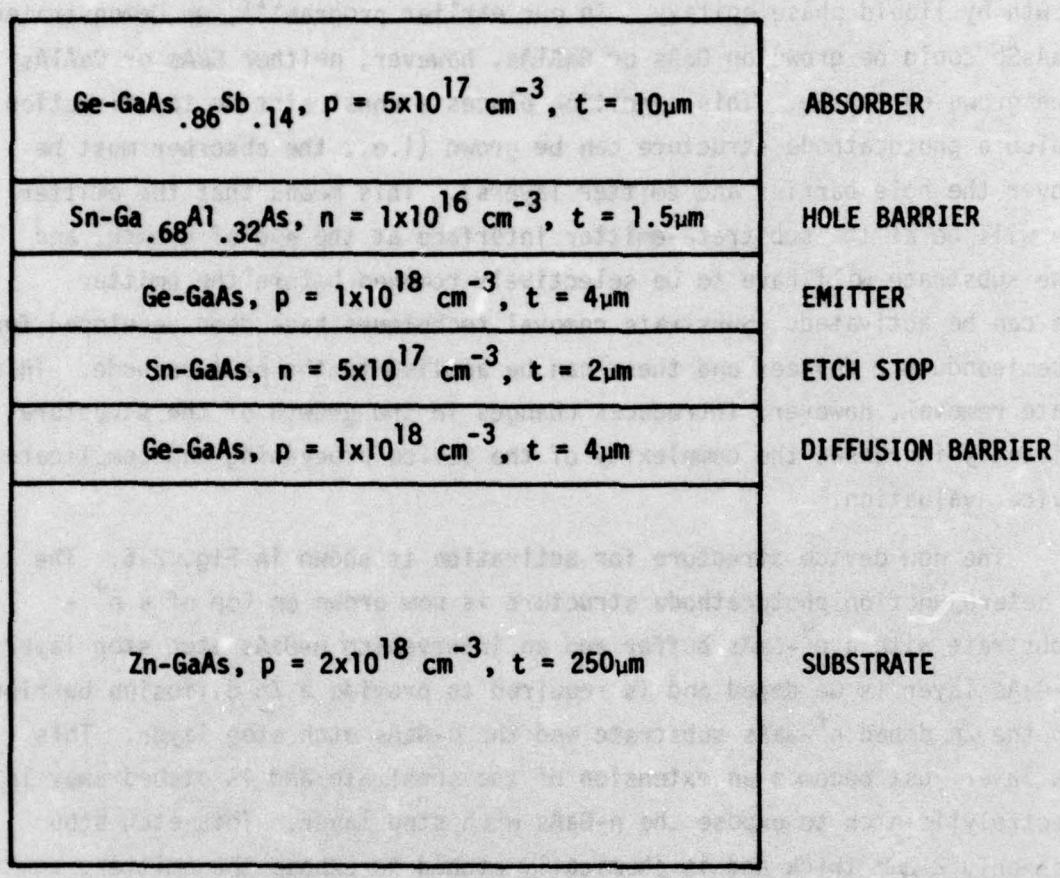



**Fig. 2.6** *Schematic diagram of the double heterojunction photocathode structure for activation. The thickness, chemical composition, dopant and carrier concentration for each layer is also shown in the diagram.*

of the device and the high temperature required in the Cs activation process.

3) Develop an activation technique which maintains the device integrity of the double heterojunction structure.

4) Demonstrate vacuum photoemission.

## 3.0 RESULTS

The goal of this research effort is to develop a complete device structure, and processing and Cs activation techniques to demonstrate field-assisted photoemission into vacuum with the double heterojunction structure in Fig. 2.6. The major efforts during the program have been in the following areas: (1) improving the growth reproducibility, (2) developing a preprocessing device evaluation technique to select the best potential structures for processing, (3) developing a processing technology to expose the emitter surface for activation and (4) developing a Cs activation technique which is compatible with active device structures. We have made considerable progress in each of these areas during this program and the first heterojunction structures (a cold cathode) were successfully Cs activated and operated. Further work is required to reach our final photocathode goal, however, the remaining problems can be well defined.

### 3.1 Materials Growth and Evaluation

The heterostructure growth procedure was described in detail in our earlier reports [1-3]. Since this has remained relatively unchanged, the steps are just listed here with only a brief description.

1) The heterojunction photocathode of Fig. 2.6 is grown in a multicompartment slider boat with 5 melt compartments. The melt compositions are each adjusted to achieve nearly exact saturation at the growth temperature (actually $\sim 2^{\circ}C$ supersaturation). The slider is then moved sequentially across the substrate with a given drop in temperature occurring during the growth of each layer. The furnace temperature at the start of the first growth is $775^{\circ}C$ and the furnace cooling rate is $1^{\circ}C$/min, with a total drop of approximately $30^{\circ}C$ during the growth of the 5 layers.
2) After removal from the furnace, any small spots of melt remaining on the surface of the substrate are removed in warm HCl.
3) The sample is cleaved along a $<110>$ plane perpendicular

to the surface and stained in the AB etch[4] to reveal the epitaxial layers. The layer thicknesses are measured from both optical and SEM photomicrographs. Further microscopic examinations are made of the surface and through the sample by IR transmission in an IR microscope to check for any gross defects or nonuniformities.

4) The energy bandgap of the absorber layer is measured by optical transmission on a Cary 14 spectrophotometer.

5) The chemical compositions of the hole barrier and absorber layers are measured by energy dispersive X-ray analysis of X-rays emitted from the sample in the SEM. The actual chemical compositions of the layers are calculated using a computer program to perform ZAF corrections[13,14] to the X-ray intensity data. The chemical composition at the interfaces is particularly examined for the formation of precipitates or signs of etchback since either of these events is a possibility when growing heteroepitaxial layers of different materials.[15] The above measurements provide a good guide for the selection of wafers for device fabrication and feedback information for better control over the materials growth parameters.

During the course of this program, there were two persistent problems that limited the growth and evaluation of heterojunction photocathode structures. The first problem was a lack of reproducibility in controlling the doping density in the hole barrier layer. The second problem was establishing the quality of each of the p-n junctions in the heterojunction structure shown in Fig. 2.6. With the earlier collector structure in Fig. 2.2, this was fairly straightforward since one could always obtain contact to the absorber and the emitter. Thus, only two junctions in series had to be evaluated. In the new structure in Fig. 2.6, only contact between the absorber and the substrate can be obtained before extensive processing and etching have been completed. Contact between the absorber and substrate place 4 p-n junctions and 2 Schottky barrier junctions in series. One is virtually assured of seeing at least back-

to-back diode behavior with all of these junctions in series and this provides no useful information on the quality of any of the individual junctions. Both of these problems have been studied in detail during this program and the results are reported.

### 3.1.1 Tin Doping of GaAlAs

As described above, one of the problems in the growth of the heterojunction photocathode was a lack of reproducibility in controlling the doping level of the GaAlAs hole barrier layer. Control over both the thickness and the free electron concentration in the hole barrier layer is absolutely essential if the device is to be operated in "punch through" to eliminate the electron barrier. This places a requirement of $t \leq 1.5\mu m$ and $n \leq 2 \times 10^{16} cm^{-3}$ on the hole barrier growth. Our design goal was to achieve a doping of $\sim 5 \times 10^{15} cm^{-3}$ for the GaAlAs hole barrier layer.

Measurements on various photocathodes indicated over an order of magnitude variation in carrier concentration in the hole barrier and often the layers were p-type. Measurements by Panish[5] indicated that the electron concentration in Sn doped $Ga_{(1-x)}Al_xAs$ decreases with increasing aluminum concentration in the region $0.3 < x < 0.5$. Since this is within the GaAsAs composition range of the hole barrier layer ($x = 0.4$), further measurements were made to study our particular system in detail. Layers of GaAlAs were grown on Cr doped GaAs substrates so that Hall effect and Schottky barrier C-V measurements could be made to measure the electron concentration. All of the GaAlAs layers were grown with a constant Sn mole fraction in the melt, $X^{\ell}_{Sn} = 0.0168$. The $Ga_{(1-x)}Al_xAs$ composition was varied over the range $0 \leq x \leq 0.4$. The results of these measurements are shown in Fig. 3.1. The very sharp drop at $x = 0.4$ clearly shows the problem in trying to achieve reproducible carrier densities at $x = 0.4$ because aluminum composition, x, can only be reasonably controlled to $\pm 0.02$. This doping variation is much sharper than that reported by Panish[5] and leads to a problem we had not anticipated.

Since the hole barrier layer composition only needs to be $x \geq 0.3$ to achieve a sufficient difference in energy gap between the emitter and hole

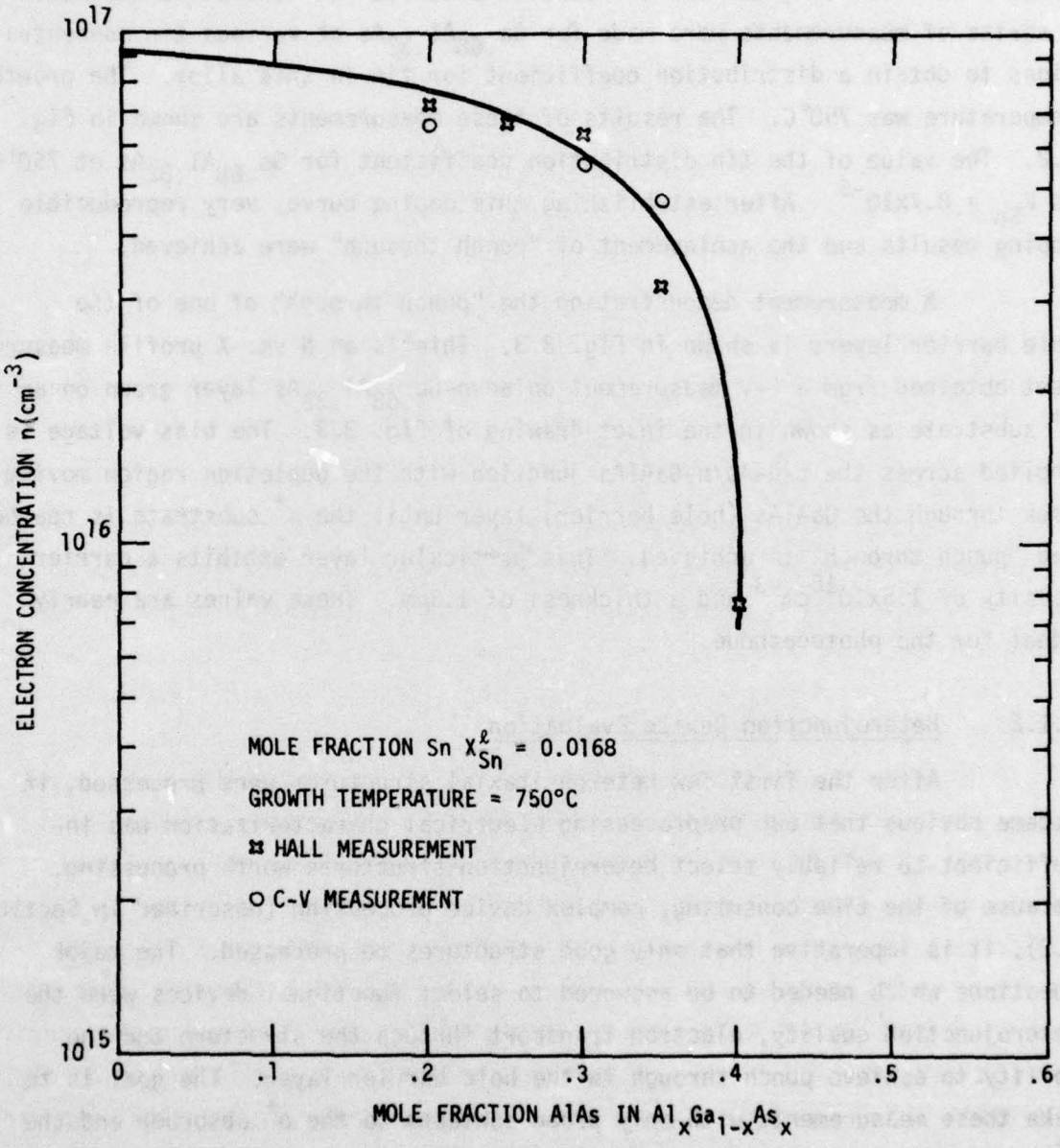



Fig. 3.1 Electron concentration vs. composition for $Ga_{(1-x)}Al_xAs$ with a constant mole fraction Sn in the melt, $S^{\ell}_{Sn}$ = 0.0168. The growth temperature is 750°C.

barrier layers, the design goal for the hole barrier composition was shifted from x = 0.4 to x = 0.32. This is sufficiently far away from the sharp break at x = 0.4 that the carrier concentration can be controlled reproducibly. A series of measurements were made for $Ga_{.68}Al_{.32}As$ at various tin concentrations to obtain a distribution coefficient for tin in this alloy. The growth temperature was 750°C. The results of these measurements are shown in Fig. 3.2. The value of the tin distribution coefficient for $Ga_{.68}Al_{.32}As$ at 750°C is $K_{Sn} = 8.7 \times 10^{-5}$. After establishing this doping curve, very reproducible doping results and the achievement of "punch through" were achieved.

A measurement demonstrating the "punch through" of one of the hole barrier layers is shown in Fig. 3.3. This is an N vs. X profile measurement obtained from a C-V measurement on an n-$Ga_{.68}Al_{.32}As$ layer grown on an $n^+$ substrate as shown in the inset drawing of Fig. 3.3. The bias voltage is applied across the p-GaAs/n-GaAlAs junction with the depletion region moving back through the GaAlAs (hole barrier) layer until the $n^+$ substrate is reached and "punch through" is achieved. This particular layer exhibits a carrier density of $1.5 \times 10^{16} cm^{-3}$ and a thickness of 1.3μm. These values are nearly ideal for the photocathode.

### 3.1.2 Heterojunction Device Evaluation

After the first few heteroepitaxial structures were processed, it became obvious that our preprocessing electrical characterization was insufficient to reliably select heterojunction structures worth processing. Because of the time consuming, complex device processing (described in Section 3.2), it is imperative that only good structures be processed. The major questions which needed to be answered to select functional devices were the heterojunction quality, electron transport through the structure and the ability to achieve punch through in the hole barrier layer. The goal is to make these measurements with only probe contacts to the $p^+$ absorber and the $p^+$ substrate of the structure in Fig. 2.6 before any mesa etching or ohmic contacts have been completed. The complication in evaluating anything at this point is that one has a device with 4 p-n junctions plus 2 Schottky junctions all in series.

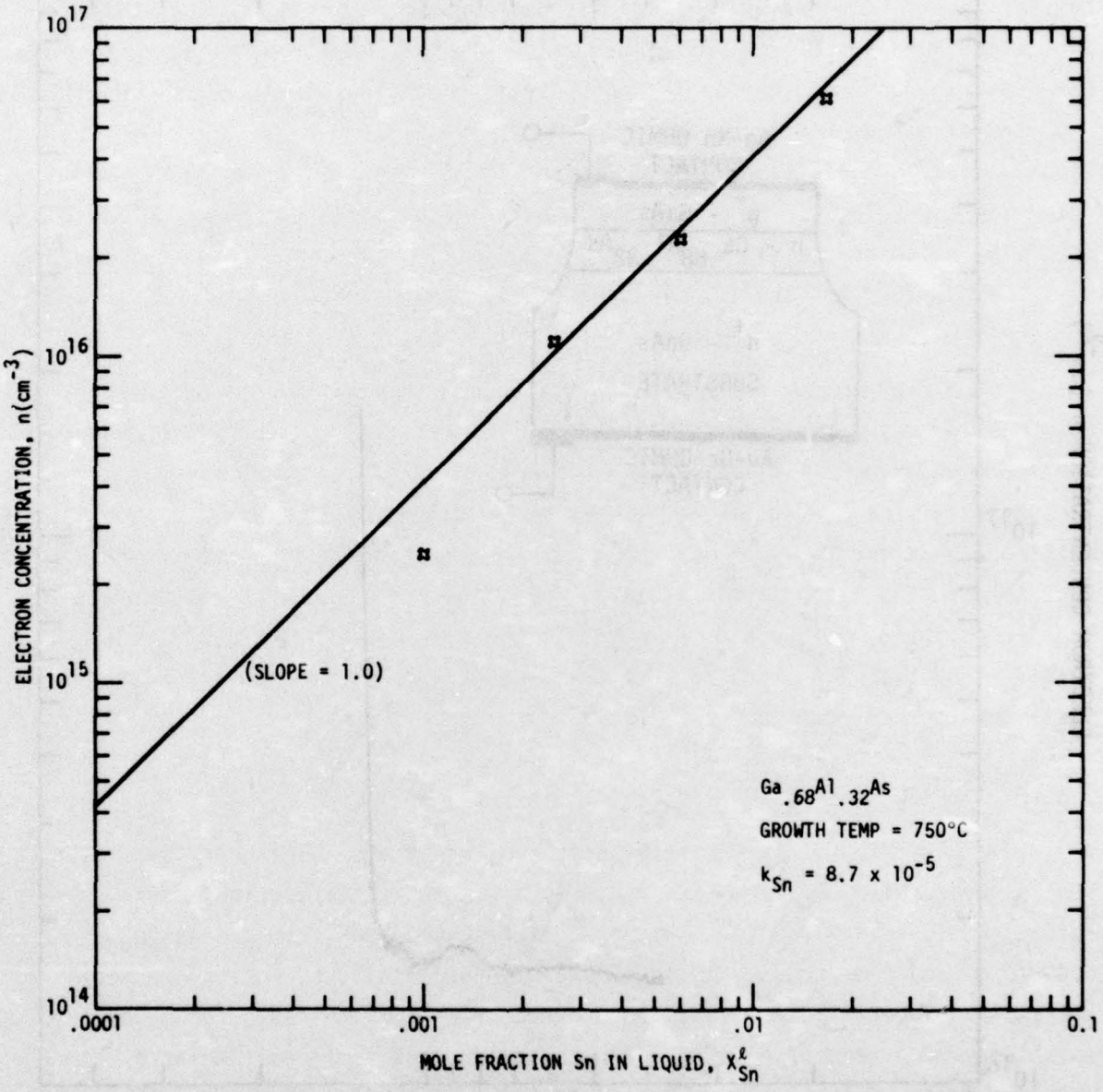



Fig. 3.2 Electron Concentration in $Ga_{.68}Al_{.32}As$ vs. mole fraction Sn in the melt. The growth temperature is 750°C.

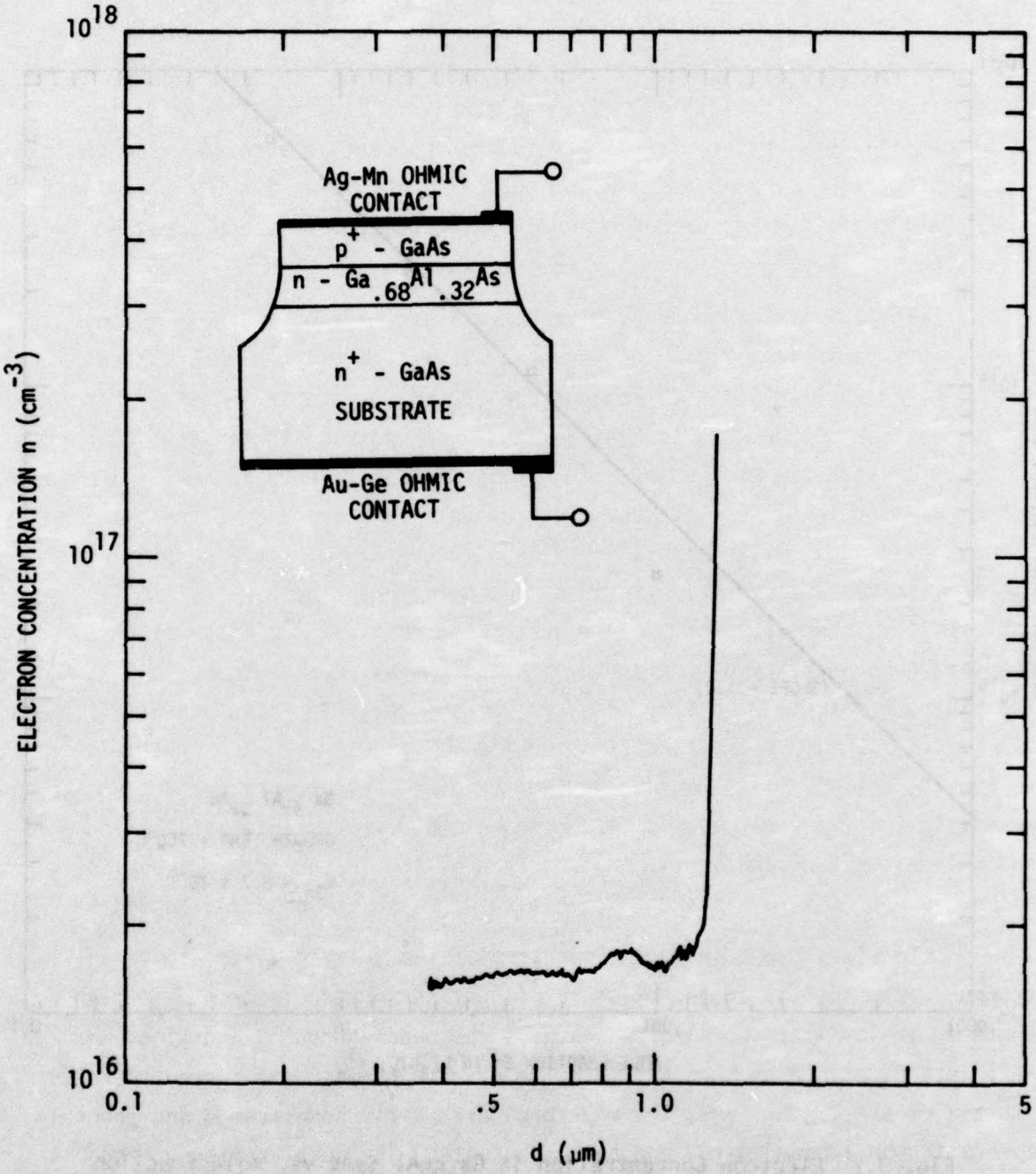



Fig. 3.3 Electron concentration vs. distance from a C-V measurement on the device shown in the inset drawing. This profile shows punch through of the n-$Ga_{68}$ $Al_{.32}As$ layer to the GaAs substrate at 15.5 volts. This is the type of hole-barrier layer required in the heterojunction photocathode.

The SEM has proven to be an extremely valuable tool in device evaluation and electron transport studies on the earlier heterojunction device structure[1-3]. With all of these junctions electrically in series, it was questionable whether the e-beam induced current in such a device could be interpreted in any meaningful way. Our earlier success led us to at least investigate these SEM measurements and they indeed provide a good deal of information for selection of good device structures.

The SEM induced current measurements are made on a piece of the 5 layer structure in Fig. 2.6 which has been cleaved on all 4 sides. These devices are irregularly sized rectangles of 20 to 50 mils in length. These samples will be referred to as "quick" diodes in contrast to those which have undergone some device processing. The quick diodes are mounted in the SEM in such a way that the finely-focused electron beam is scanned across a cleaved face with the edge of the junctions exposed at that face. At any point where the beam strikes the sample, a large number of electron-hole pairs are generated in a semi-spherical volume just below that point. This volume is dependent on the energy of the incident electrons as well as the material parameters, but is between 1 and 3μm for our system. The excess carriers in this small volume then drift, diffuse or recombine just like any other excess carrier in their position would. Any motion of these carriers creates a current in the external circuit connected to the device. This external current is displayed on the same oscilloscope screen as the secondary electron image so that each of the layers and the junction currents are observed together.

To study the transport properties of the 5 layer photocathode structure, the quality and/or presence of junctions, the electron diffusion length in the emitter and absorber layers, the punch-through condition, and the existence of energy band barriers, we observe the induced current wave form. With all of these junctions, the waveforms are fairly complicated and strongly dependent upon e-beam energy and beam scan rate. The accelerating voltage is always a compromise between a low value which provides good spatial resolution and good junction current separation, and a high value which increases the junction currents because of reduced surface recombination. The scan rate is chosen to give the optimum response in the external induced current and is

strongly effected by the doping densities of the various layers and the device size because of the coupling capacitance effect of all the junctions in series.

A typical secondary electron (SE) micrograph with a super-imposed induced current (IC) line scan for a quick diode is shown in Fig. 3.4(a). The dark regions are the n-type layers which have a lower SE yield than the p-type layers and, therefore, appear dark in the SE image. The layer on the left (larger IC peaks) is the hole barrier layer while the one on the right is the etch stop layer. The line scan and SE image both clearly show the 4 p-n junctions (the p-n junctions are at either positive or negative peaks in the IC). Since the IC peaks and the SE contrast lines are coincident, the p-n junctions and metallurgical junctions are coincident.

Examination of the IC with applied bias reveals further information about the device structure. The IC line scans at -10, 0 and +10 V applied to the absorber are shown in Fig. 3.4(b). These are taken from a separate oscilloscope so no SE image is available. The +10 V trace (lower one) shows that the electron diffusion length in the emitter is sufficient to allow transport of electrons clear across the emitter (i.e., the IC tails off exponentially from the HB-E junction and does not become zero until right at the etch stop layer). Careful examination of these three IC traces reveals that punch through is not achieved. On both the +10 V and -10 V traces, there is still a very small region in the trace where the current changes polarity (this occurs where either the positive or negative zero bias peaks are located). In samples where punch through is achieved, the current becomes absolutely unipolar with sufficient applied bias.

An example of good punch through character is shown in the IC traces of Fig. 3.5(a) and (b). Fig. 3.5(a) shows a sequence of increasing steps of negative bias applied to the absorber until punch through is reached at -12 V. (This is the bias polarity for device operation.) Fig. 3.5(b) shows the same device with positive bias applied until punch through is achieved in the reverse direction. Note particularly in Fig. 3.5(b) that it is very easy to see the small positive peak just to the left of the major negative peak become smaller with each step in the bias until at the very top, absolutely no positive peak

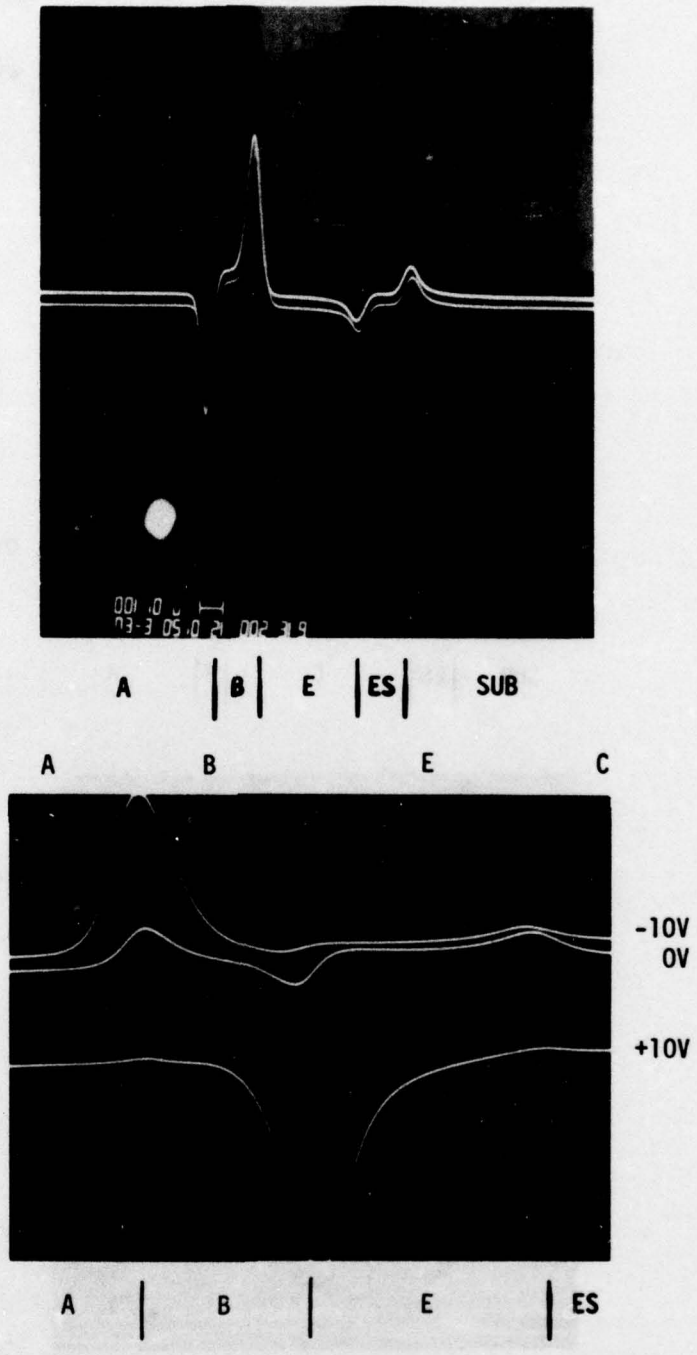
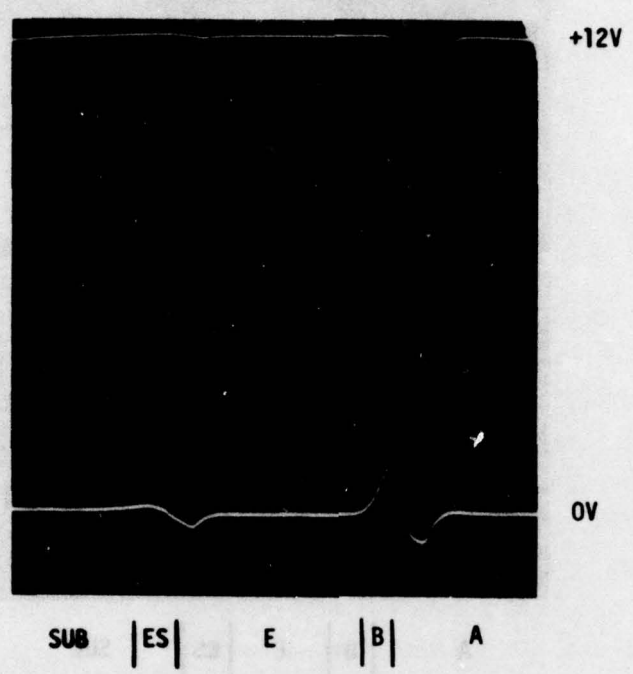



Fig. 3.4 Secondary electron (SE) micrograph and induced current (IC) trace from a cross-section of a heterojunction structure similar to that shown in Fig. 2.6. (a) SE micrograph with superimposed IC trace at zero bias. (b) IC traces with increased magnification and -10, 0, and +10 volts bias applied to the absorber. Note that under + or -10 volts bias, the depletion region has not moved completely across the hole barrier layer (i.e. punch through is not achieved).



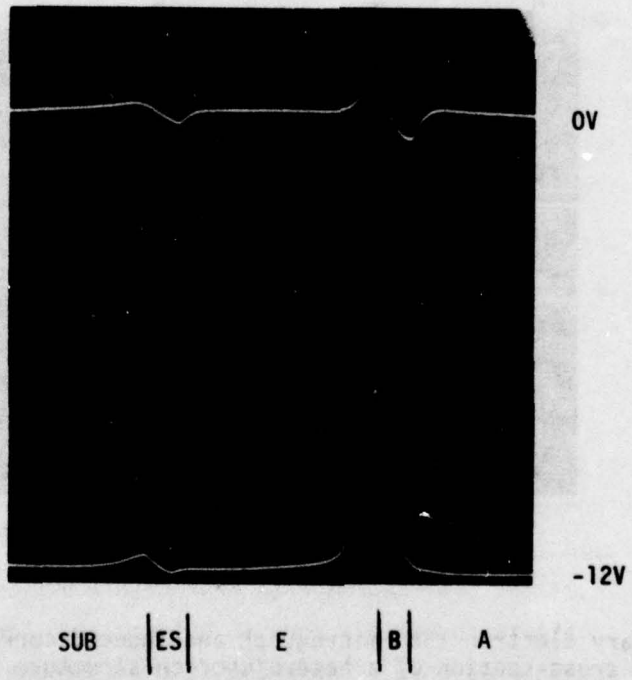




Fig. 3.5 The induced current (IC) trace for a structure similar to that in Fig. 3.4 except the punch through condition is achieved. a) Induced current trace for a sequence of increasing steps of negative bias applied to the absorber; b) The same as a) except for a positive bias applied to the absorber. In both polarities, the positive or negative peak in the induced current extends completely across the hole barrier layer.

is observed. Approximately 5 V beyond punch through, (17 V total), can be applied before the onset of high hole injection. This is the type of IC measurement one looks for in selecting a device suitable for processing.

Another problem frequently observed in these devices has been either a p-type hole barrier layer or one which is punched through at zero bias. An example of this is shown in Fig. 3.6. In this case, the zero bias IC trace is not symetrical (i.e., a positive and negative peak) through the hole barrier layer as it is across the etch stop layer. This unipolar behavior in the hole barrier always remains in the same polarity with both positive and negative bias because there is no p-n junction. Measurements like this led to the Sn doping study described in Section 3.1.1 so that reliable doping and junctions could be achieved.

The SEM induced current measurements are indeed a powerful tool in examining very complicated heterojunction structures. The measurement is now done routinely on every single structure to determine its potential before making any significant investment into processing the device.

## 3.2 Photocathode Device Processing

All of the prior processing techniques[1-3] were developed to produce a structure (Fig. 2.2) which could be tested for internal photoemission in order to demonstrate the feasibility of a double heterojunction field-assisted photocathode.

In this program, the goal of the processing research is to develop a technique to fabricate a useful device appropriate for Cs activation from the layered structure shown in Fig. 2.6. This involves a major difference with respect to the previous processing, since the new device must have the emitter exposed for Cs activation. The approach to fabricate a device was to first bond the sample (substrate down) to a ceramic holder, and then to remove the substrate in the active area only by thinning it down through a tapered hole in the ceramic. This would then expose the emitter surface for Cs activation over a limited area. Fig. 3.7 shows a schematic diagram of the processed device structure. The ceramic chip is fabricated to accommodate four devices, so that

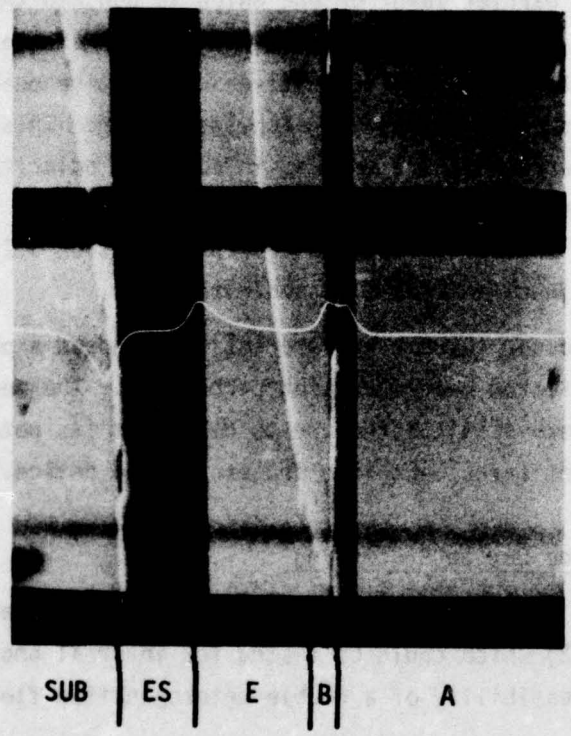



Fig. 3.6 Secondary electron (SE) micrograph with superimposed induced current (IC) trace for a structure similar to that in Fig. 3.4 except that the zero bias IC is not symmetrical. This indicates that the hole barrier layer is punched through at zero bias.

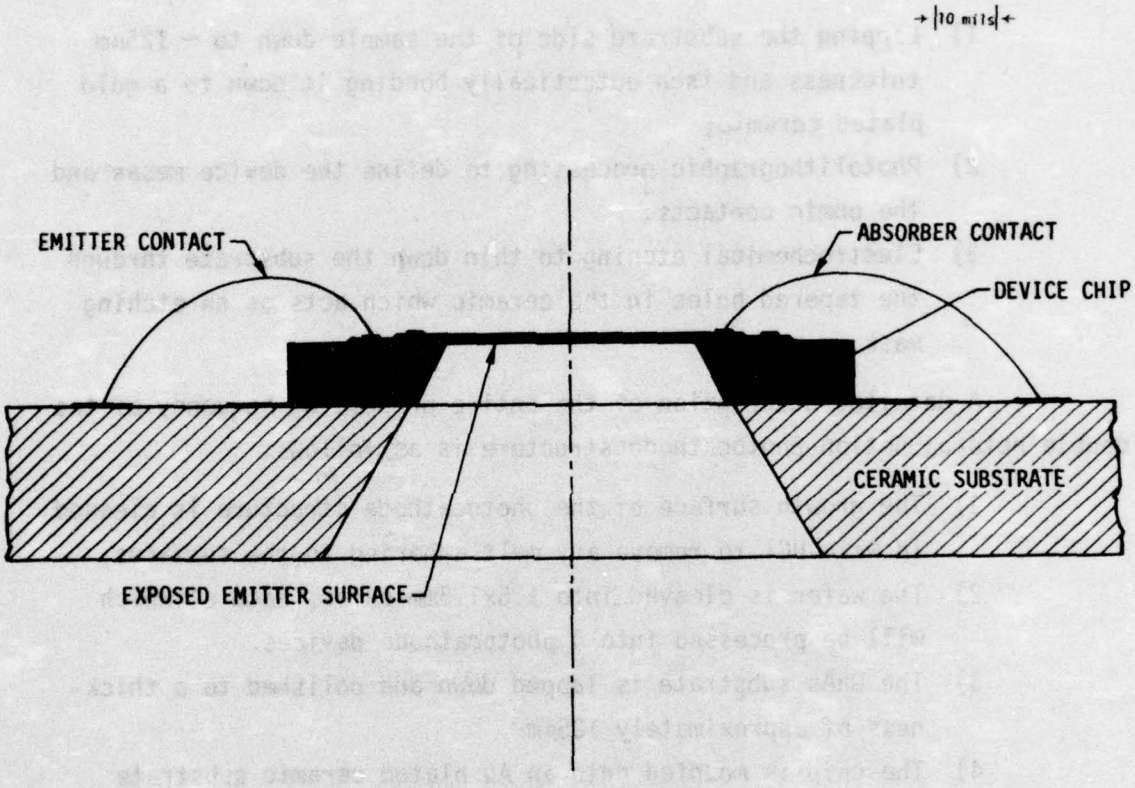



Fig. 3.7 Schematic diagram of the double heterojunction photocathode showing the planned mounting, bonding and substrate removal required to produce a device for Cs activation.

after bonding, all four devices are processed simultaneously.

The photocathode structures are fabricated from wafers selected on the basis of the above SEM evaluation and which are structurally suitable to our processing technique. The processing can be divided into three major areas:

1) Lapping the substrate side of the sample down to ~ 125μm thickness and then eutectically bonding it down to a gold plated ceramic;
2) Photolithographic processing to define the device mesas and the ohmic contacts;
3) Electrochemical etching to thin down the substrate through the tapered holes in the ceramic which acts as an etching mask.

A detailed description of the entire processing sequency of the double heterojunction photocathode structure is as follows:

1) The growth surface of the photocathode structure is cleaned in warm HCl to remove any melt adhering to the surfaces.
2) The wafer is cleaved into 1.5x1.5mm chips, each of which will be processed into 4 photocathode devices.
3) The GaAs substrate is lapped down and polished to a thickness of approximately 125μm.
4) The chip is mounted onto an Au plated ceramic substrate which has 4 tapered holes which are in the same pattern as all of the mesa and contact masks. An eutectic bond is formed between the Au plated ceramic and GaAs by heating to 500°C for 5 min.
5) The device mesa shown in Fig. 3.7 is defined using a photoresist mask and Br-methanol etchant. The etching continues until the substrate is reached.
6) The sample is cleaned to remove the photoresist.
7) The absorber mesa is defined using a photoresist mask. The $p^+$-GaAsSb layer (the absorber layer) is selectively removed

using $H_2O_2$:$NH_4OH$:$H_2O$ solution as a selective etchant.

8) The $n^-$-GaAlAs (the hole-barrier layer) is removed in a selective etch of $H_2O_2$:$NH_4OH$:$H_2O$ until the emitter layer is just exposed.

9) The sample is cleaned again and another photoresist is applied to define the contact areas for the p-GaAsSb (A) and $n^-$-GaAs (E).

10) The ohmic contact metallization is deposited on both the absorber and emitter surfaces. Ag-Mn is first deposited by e-beam evaporation, then a small bonding pad area is defined and W+Ti+Au are sequentially sputter deposited on top of the Ag-Mn.

11) Au wires are bonded to the absorber and emitter contact areas.

12) The GaAs substrate is now thinned down to expose the emitter surface for the activation process. The substrate thinning is done in a KOH electrolytic etch. This etch is performed in selected areas using the ceramic substrate hole pattern as the etch mask.

At this point, the device is completed and ready for Cs activation as described in Section 3.4.

Many of the above steps have been developed earlier and are described in the earlier reports.[1-3] However, there are several new problems which arose because of the necessity to expose the emitter and to heat the sample to the heat cleaning temperatures required for activation (~ 610°C).

One of the problems which we examined in considerable detail is the etch thinning of the GaAs substrate. The complete etching process consists of a three-stage etching technique. The $p^+$ substrate is first partially removed by a chemical etch. The last of the substrate is removed by the KOH electrolitic etch, which is a selective etch that stops when the $n^-$-GaAs etch stop layer is reached. The etch stop, ES, layer is subsequently removed by the third stage chemical etching to expose the active $p^+$-GaAs emitter surface of the DH-photocathode device. The electrolytic etch must be very carefully regulated so that no islands are left isolated by current crowding effects.

A low current density (80 ma/cm$^2$) was found to maximize the differential etching ratio between p and n type GaAs. This results in good control on the etch stop when the n-GaAs layer is reached. It is also important to maintain a steady current density throughout the etching process to avoid islands. In our case, since the etching is performed through small holes in the ceramic, some undercutting occurs during the etching and the surface area of the $p^+$-substrate exposed to the electrolytic changes as the etching proceeds. Best results were obtained by increasing the etching current in steps from time to time to compensate for the increased surface area.

Fig. 3.8 shows a photograph of a hole electrolytically etched in the GaAs substrate through a 1mm diameter hole in the ceramic. This figure shows that the etch stops perfectly at the n-GaAs layer. The shape of the hole is elliptical rather than circular like the mask. This is due to the orientation dependence of the etch-rate. Along the smaller axis, the etching rate is slower than the vertical etch rate, while the opposite is true for the longer axis. The sides of the hole show an abrupt and steep slope along the narrow region, where the undercutting is minimal and the vertical etching rate is faster, and a gradual slope along the wide region where the undercut is of the order of the thickness etched, and the etching rate is slow. The bottom of the hole is perfectly flat. After the n-stop layer is chemically etched to expose the p-GaAs emitter, the final surface has a good polished and flat finish. The three stage process devised for selective etching of the substrate works very well and is under very good control. One problem noted on these photocathode structures is that they are quite fragile. They are easily broken during cleaning or any operation where they receive some type of mechanical shock.

One of the remaining technical problems regarding the photocathode structure, is its ability to withstand the high temperature heat treatment and thermal cycling which are required in the Cs activation process. To study this problem, we first examined some of the p-n junction test photocathode devices (devices like that in Figs. 2.1 and 2.2 which were used in the previous program) under similar thermal tests. Fig. 3.9 presents a photograph of a photocathode device and its I-V characteristics before and after heat treatment at 610°C

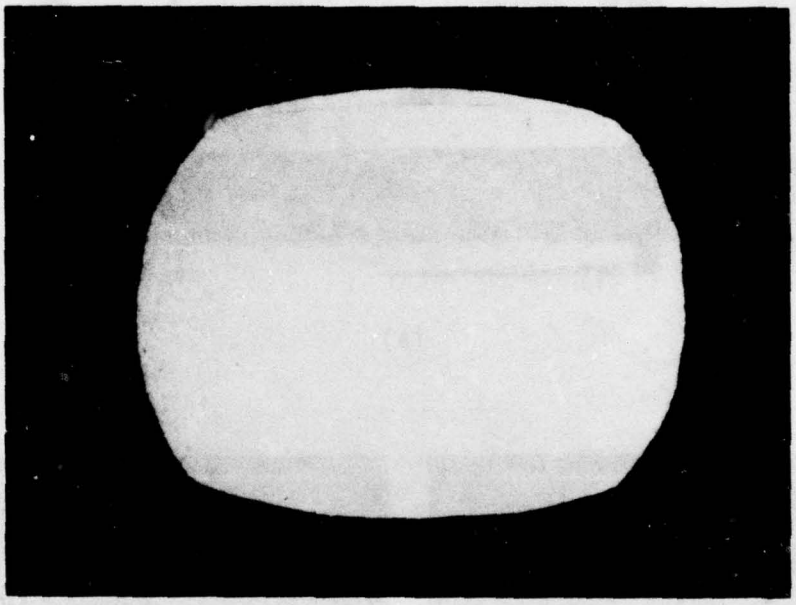
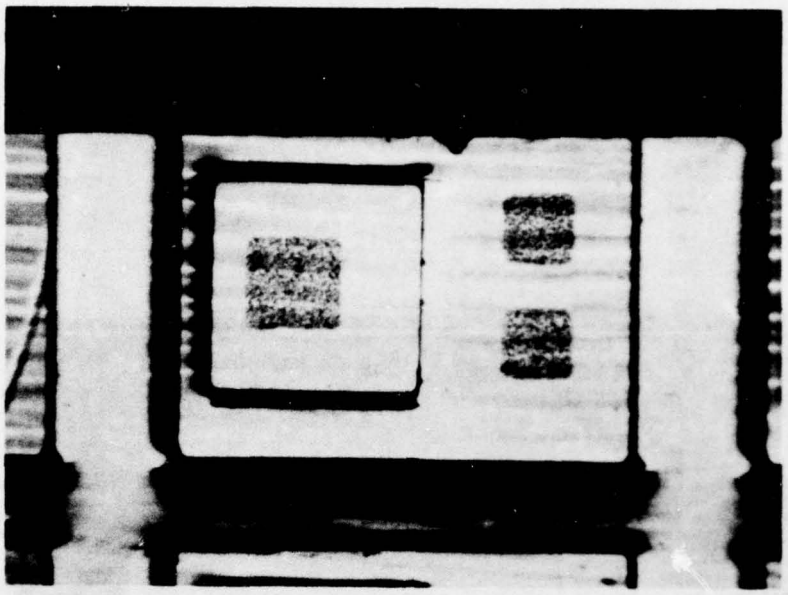
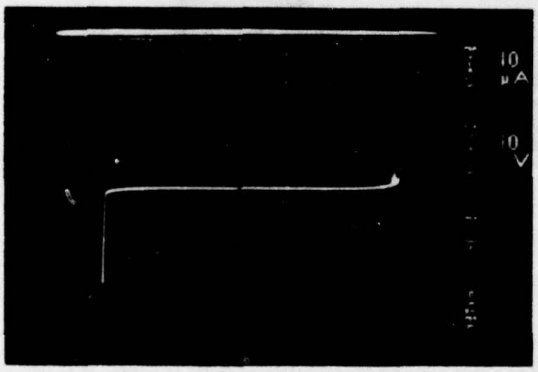


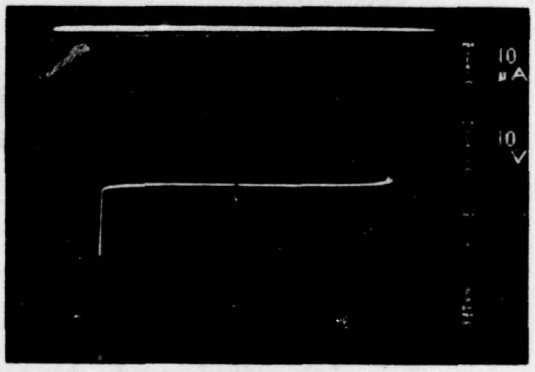
Fig. 3.8 Photograph showing the top view of a hole etched in the GaAs substrate through a 40 mils diameter hole after the first two stages. The etching stopped flat at the n-GaAs layer.



(a)




(b)




(c)

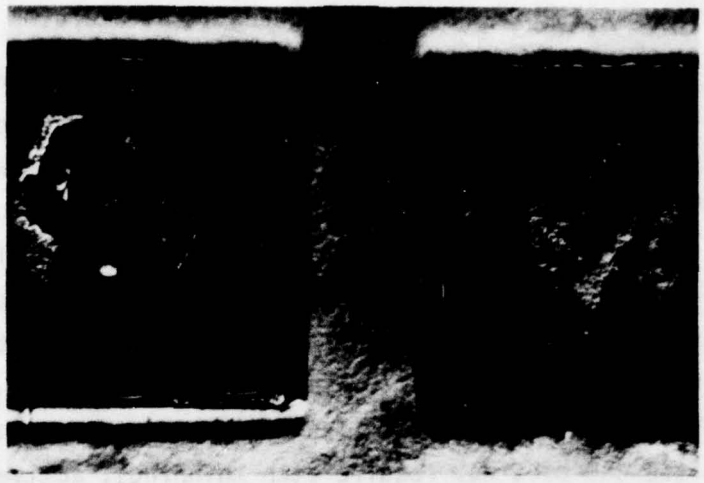
Fig. 3.9 (a) Photomicrograph of heterojunction photocathode after heat treatment of 610°C for 60 sec. (b) I-V characteristic of above device between absorber and emitter before heat treatment. (c) I-V characteristic after 60 sec heat treatment. Note that both the breakdown voltage and the leakage current were unaffected by the heating.

for 60 seconds. As can be seen in the I-V characteristics, both the breakdown voltage and the leakage current remained unchanged, therefore, the devices can certainly withstand the heat cleaning temperature.

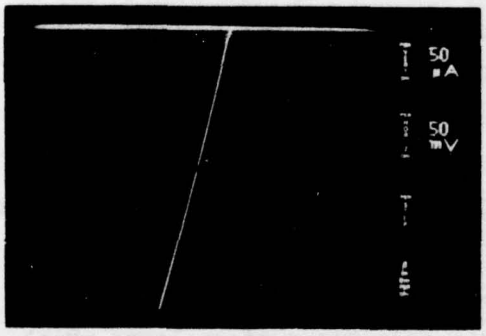
Because of the complex processing requirements of the double heterojunction photocathode, we decided that initial activation experiments should be carried out on a GaAlAs-GaAs "cold cathode." In this way we could study the Cs activation of a heterojunction device on a much simpler structure. The cold cathode device structure is shown in the Fig. 3.25. This device comes close to simulating the operation of the photocathode because the n-$Ga_{.7}Al_{.3}As$ and $p^+$-GaAs are grown of the identical composition, doping densities and thickness as the hole-barrier and emitter layers in the photocathode structure. The devices would be mounted in the same fashion as the photocathode (except the emitter is on top and does not require etch thinning), activated and then measured to study the Cs activation processing and its effects on the I-V characteristics of the heterojunction.

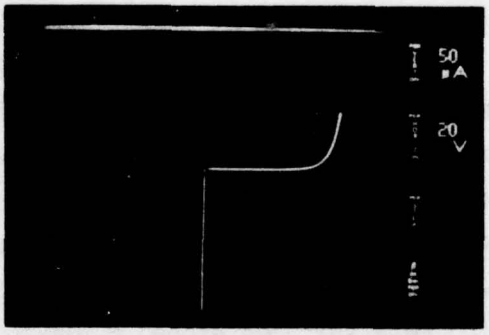
When the first diodes were fabricated, our Cs activation chamber was not yet in operation at the Science Center, so these devices were sent to Dr. John Pollard at Night Vision Labs (NVL) for activation. All of the first set of devices became shorted during the heat cleaning required for Cs activation. A series of measurements were made where the sample was heated to successively higher temperatures in 50°C intervals with cooling back to room temperature and a check of the I-V characteristic between each heating. Nearly all of the diodes became shorted at ~ 450°C. The diodes were removed from the chamber and the mesa surfaces etched ~ 5μm to remove any possible surface layer which could short the junction. The junction still remained as short. The 450°C temperature suggests that possibly the Au wire bond is the source of trouble because there is a Au-Ga eutectic at 455°C[12]. With a large source of Au available at the Au ball bond, an eutectic liquid forms which dissolves away enough GaAs to go completely through the p-n junction and create the short.

Two identical mesa samples were prepared for heat treatment. One was prepared with the usual Au wire bond, the second was probed with a 5 mil W wire. A photograph of the two samples after heating to 610°C for two minutes is shown in Fig. 3.10. The Au wire bonded sample on the left shows



(a)




(b) (c)

Fig. 3.10 (a) Photomicrograph of GaAlAs-GaAs cold cathodes after heating to 610°C for 2 min. The device on the left was bonded with a Au wire and shows signs of eutectic liquid formation and crystal regrowth. The device on the right was probed with a W wire and does not exhibit any contact degradation. The I-V characteristics for the Au bonded and W probed diodes are (b) and (c) respectively.

distinct regions in the upper right corner where a 120° intersection occurs in the contact. This is a characteristic feature of liquid formation and crystal regrowth. The I-V characteristics of the two diodes are shown in Fig. 3.10(b) and (c) after the heat treatment. This test clearly shows that the Au contact wire is the source of the problem and that the contacting technique would have to be changed to a probe type of contact or else the ohmic contact would have to include an inner metallic layer which prevented the Au-Ga eutectic formation under the Au wire bond.

To find an appropriate metal for such an inner layer, we examined the possible Ga binary phase diagrams in Hansen [12] and found that several refractory metals were good candidates. We first tried W which proved successful. In all of our measurements, W acted as a perfect barrier to Au alloy formation and movement into the GaAs layer. A photograph of a cleaved cross-section of two GaAs substrates which were eutectically Au bonded is shown in Fig. 3.11. One substrate (a) is shielded against Au eutectic liquid formation with a layer of W. The other substrate (b) is unprotected. As shown in the photograph, the 5μm of Au between the two substrates formed an eutectic liquid with the unprotected substrate (b), and moved into the sample to a depth of ~ 25μm while the W-coated substrate (a) remained unaffected.

These processing steps have now been incorporated into our photocathode and cold cathode processing. The results of preliminary Cs activations on these devices indicate that the contact problem is under control with the above contacting technology.

## 3.3 Heterojunction Device Studies

As described in Section 2.1, the review of our earlier program, one of the problems demonstrated by the p-n junction collector photocathode structure was that while excellent internal transport efficiency could be obtained with this heterojunction device, the external 1.06μm quantum efficiency was quite low. This low efficiency is due to an adverse bandgap grading at the absorber-hole barrier junction. The adverse grading effect was quantitatively measured by an optical deconvolution technique from optical transmission data[6] on a GaAlAs-GaAsSb heterojunction. The calculated energy gap vs. distance

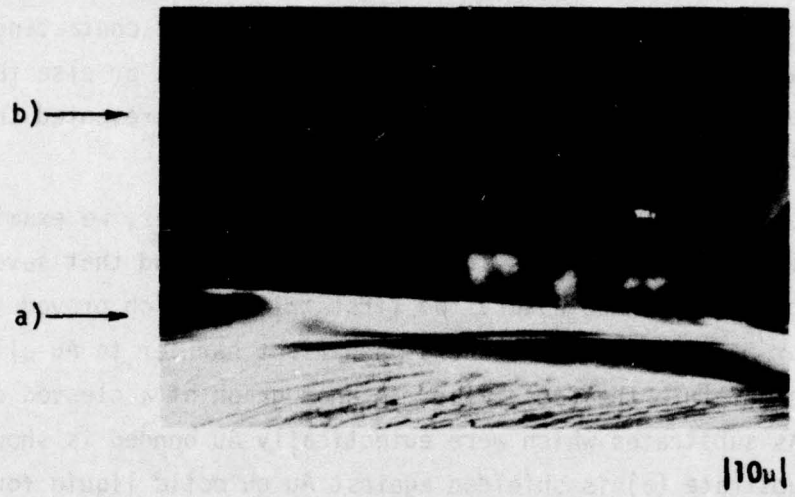



Fig. 3.11 Photograph of a cleaved package of two substrates of GaAs which were eutectically bonded: a) this substrate is protected by a sputter deposited W layer, on top of which there is a Ti layer (~ 500Å) and Au (~ 5μm); b) the unprotected substrate. The photomicrograph clearly shows the deep Au penetration into the upper unprotected GaAs substrate.

profile and the inferred energy band diagram at the absorber-hole barrier (A-B) junction are shown in Fig. 3.12.

We see that the initial grading in the GaAsSb is very rapid. The bandgap changes from 1.4 eV at the interface to 1.22 eV a .5 micron from the interface. After .5 micron the grading is very slow. The energy band diagram shows that in addition to an adverse built-in electric field in the bulk of the GaAsSb layer there is a sharp potential hump at the interface. Detailed studies of the optical and electron transport properties of this A-B junction reveal that the potential hump is far more serious in limiting the 1.06$\mu$m response than the adverse bulk grading away from the junction.

Photoresponse and optical transmission measurements were made on a number of GaAlAs-GaAsSb (A-B) heterojunctions which were grown under a variety of growth conditions (growth temperature, cooling rate, temperature gradient, melt supersaturation, etc.). These different growth conditions all effected the composition and bandgap grading, however, none was successful in eliminating the potential hump at the interface. All of the photoresponse curves looked like that of $I_a$ in Fig. 2.3.

The reason that this hump cannot be eliminated is that lattice constant pulling[8,9] prevents the immediate growth of the thermodynamic equilibrium composition GaAsSb layer on either GaAs or GaAlAs. Thus, the initial growth is always GaAs, which grades to the equilibrium GaAsSb alloy over a distance between 0.3$\mu$m and 10$\mu$m or more depending on the growth conditions. In no case have we been able to reduce this grading to less than 0.3$\mu$m. Because the p-GaAsSb absorber must be heavily doped with respect to the n-GaAlAs hole barrier in order to deplete the hole barrier, this 0.3$\mu$m grading region can never be pulled within the depletion region. The only solution to this problem is to grow two distinct layers; one a graded layer which will be in the depletion region and a second constant composition layer. The graded GaAsSb region must be doped either very lightly n-type or p-type while the constant composition GaAsSb layer is more heavily doped p-type. Placing this graded layer within the depletion region eliminates the barrier problem because the energy band profile is dominated by the depleted charges at the junction rather than the energy bandgap grading. A comparison of the

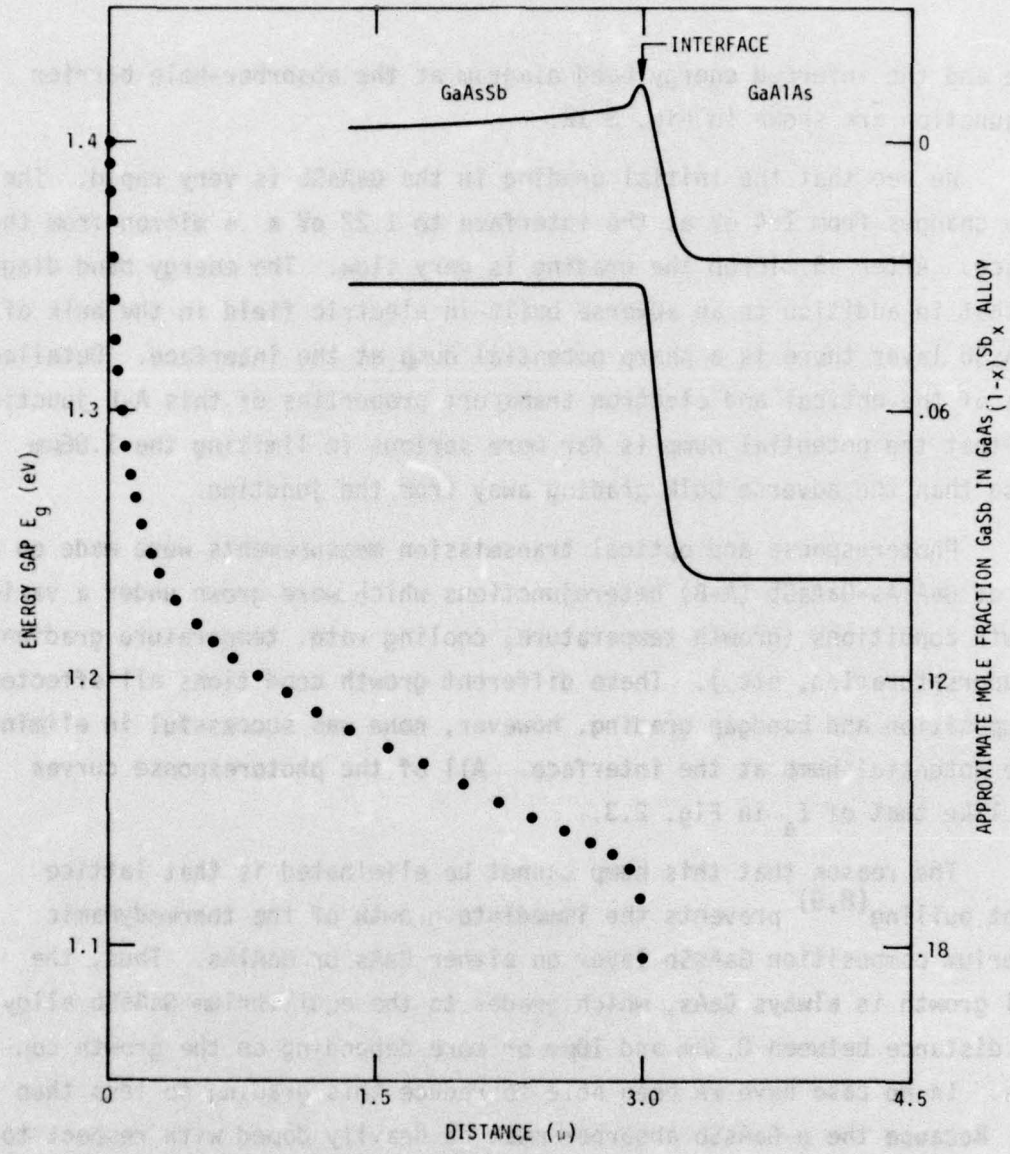



Fig. 3.12 Bandgap grading of the GaAsSb layer. The insert shows the energy band diagram for the absorber hole barrier junction at zero bias.

normal and modified A-B junction energy band diagrams is shown in Fig. 3.13. The modified version should clearly show a photoresponse dependent only on the absorption coefficient in the absorber.

The potential of the above structure to achieve uniform wavelength response has been demonstrated by growing the two structures shown in Fig. 3.13 and comparing their photoresponse. Both structures were grown from the same melts under identical conditions, the only difference being that the new structure had a 3rd melt placed between the first and second melts in the original structure to provide the added n-GaAsSb inter-layer. The optical transmission data T, and the optical absorption A = (1-T) shown in Fig. 3.14(a) are identical for both structures. The photoresponse for each structure is shown in Fig. 3.14(b). Curve A is nearly identical to all of our measurements of photocathode photoresponse (Fig. 2.3) which exhibits a poor long wavelength efficiency. Curve B for the new structure shows a perfectly flat topped response and the long wavelength tail is a mirror image of the optical absorption tail in Fig. 3.14(a) indicating that the response is now solely controlled by the composition and absorption of the $GaAs_xSb_{1-x}$ absorber.

This multiple layer approach has not been incorporated into the heterojunction photocathode during this program because of the added growth complexity and our major goal is to demonstrate vacuum photoemission rather than peak 1.06$\mu$m sensitivity. The above photodiode experiment, however, clearly demonstrates that the extra graded layer will solve the poor long wavelength efficiency problem.

## 3.4 Cs Activation Studies

The $p^+$-GaAs electron emitter layer of the heterojunction photocathode shown in Fig. 1.1 must be brought to a condition of negative electron affinity (NEA) for proper device operation (NEA occurs when the conduction band of a semiconductor lies below the vacuum level at the semiconductor surface). In semiconductor photoemitters, the absence of NEA means that bulk generated thermal photoelectrons will have a very low probability of escape after diffusing to the photocathode surface. NEA can be achieved on $p^+$-GaAs by treatment with Cs and O in an ultra high-vacuum environment. The Cs activation procedure

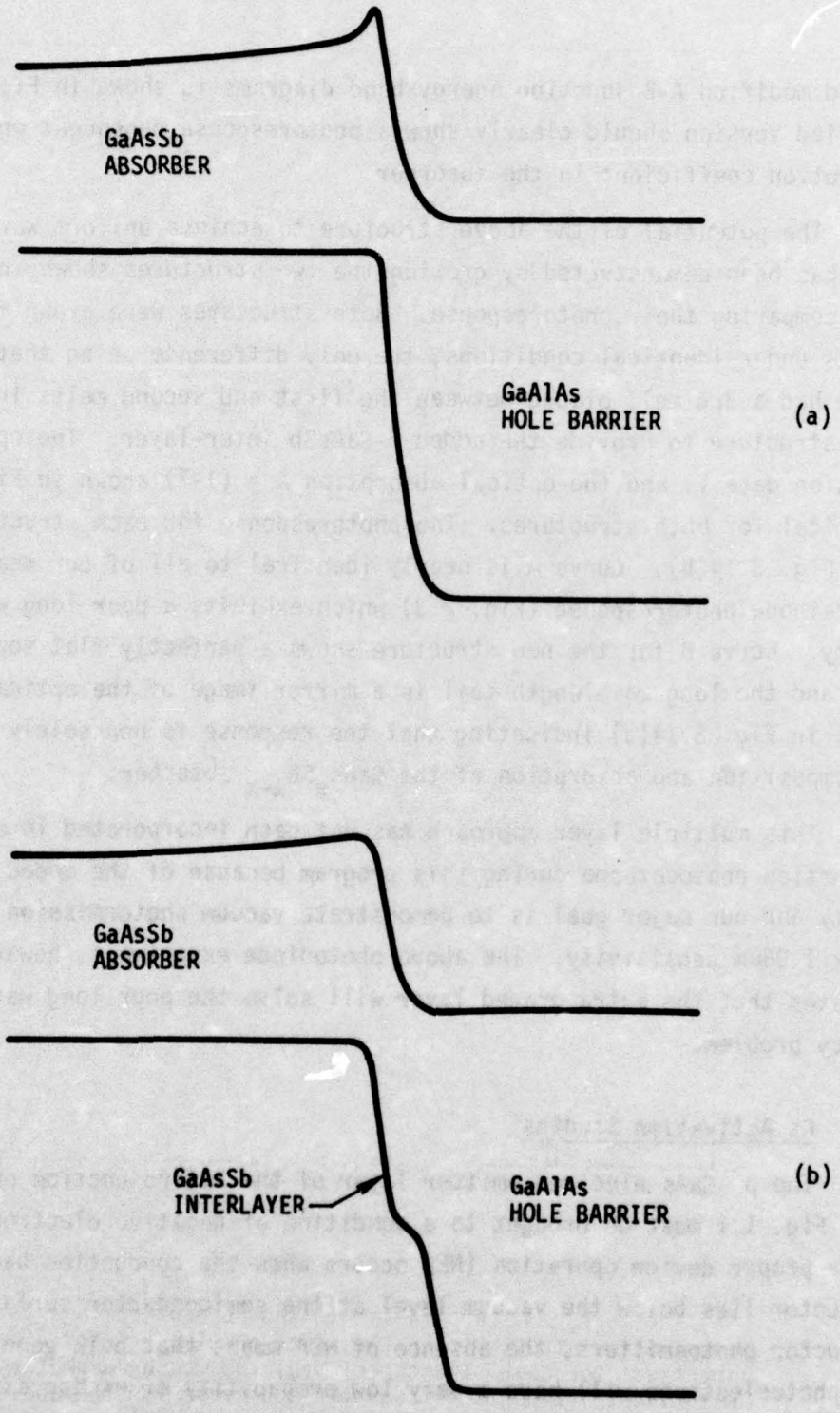



Fig. 3.13 The energy bands at the absorber-hole barrier junction. (a) The present 2 layer junction of p-GaAsSb/n-GaAlAs and (b) The new 3 layer structure of p-GaAsSb/n-GaAsSb (graded)/ n-GaAlAs.

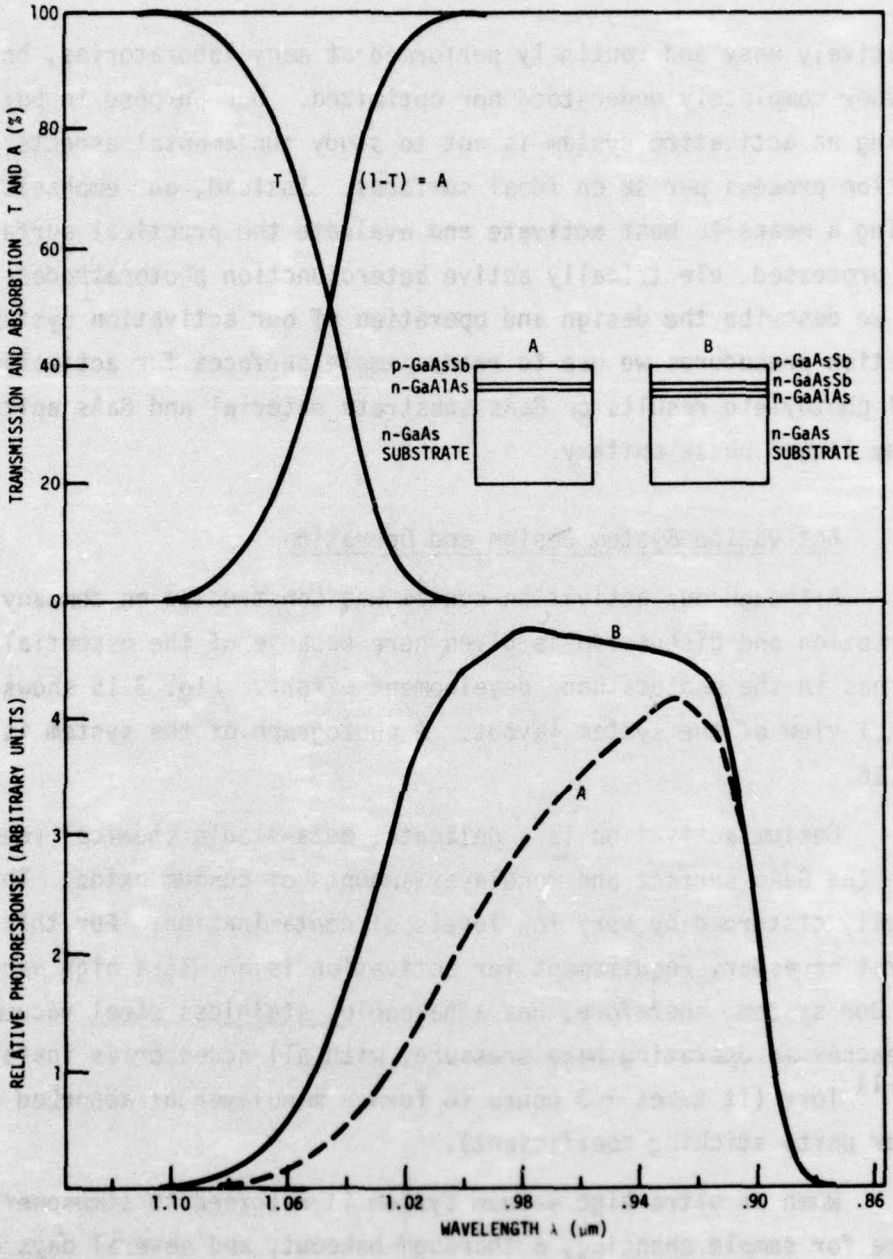



Fig. 3.14 (a) The measured transmission T, and absorption (A = 1-T) for the two structures in the inset drawing. T and A were identical for both structures. (b) The measured photoresponse with light incidents through the substrate for the above two structures. Curve A is a mirror image of the photocathode response in Fig. 2.2 which has the same absorber-hole barrier junction. Curve B is for the new absorber-hole barrier structure and clearly demonstrates the improved long wavelength response.

is relatively easy and routinely performed at many laboratories, however, it is neither completely understood nor optimized. Our purpose in building and operating an activation system is not to study fundamental aspects of the activation process per se on ideal surfaces. Instead, our emphasis is on providing a means to best activate and evaluate the practical surfaces found on our processed, electrically active heterojunction photocathodes. In this report we describe the design and operation of our activation system, the preparation procedures we use to ready sample surfaces for activation, and initial photoyield results on GaAs substrate material and GaAs epitaxial layers grown by liquid phase epitaxy.

### 3.4.1 Activation System Design and Operation

Although our activation system was constructed on company IR&D funds, a description and discussion is given here because of the essential role this system has in the photocathode development effort. Fig. 3.15 shows a cross-sectional view of the system layout. A photograph of the system is shown in Fig. 3.16.

Cesium activation is a delicate, meta-stable chemical reaction between the GaAs surface and monolayer amounts of cesium oxide. This reaction is readily disturbed by very low levels of contamination. For this reason, the first necessary requirement for activation is an ultra high vacuum environment. Our system, therefore, has a bakeable, stainless steel vacuum chamber that reaches an operating base pressure, with all accessories installed, of $\sim 3\times10^{-11}$ Torr (it takes ~ 3 hours to form a monolayer of absorbed gas at $10^{-10}$ Torr for unity sticking coefficient).

When an ultra high vacuum system is returned to atmospheric pressure for sample changing, a thorough bakeout, and several days of continuous pumping are required to once again return to the $10^{-11}$ Torr range needed for activation. To allow the rapid cycling of samples, avoid a time bottleneck in the evaluation of devices and maintain the low base pressure performance of the system, we designed an air-vacuum interlock mechanism having a loading chamber separate from the main vacuum chamber. Using the interlock we can load electrically active devices mounted on a holder without venting the main

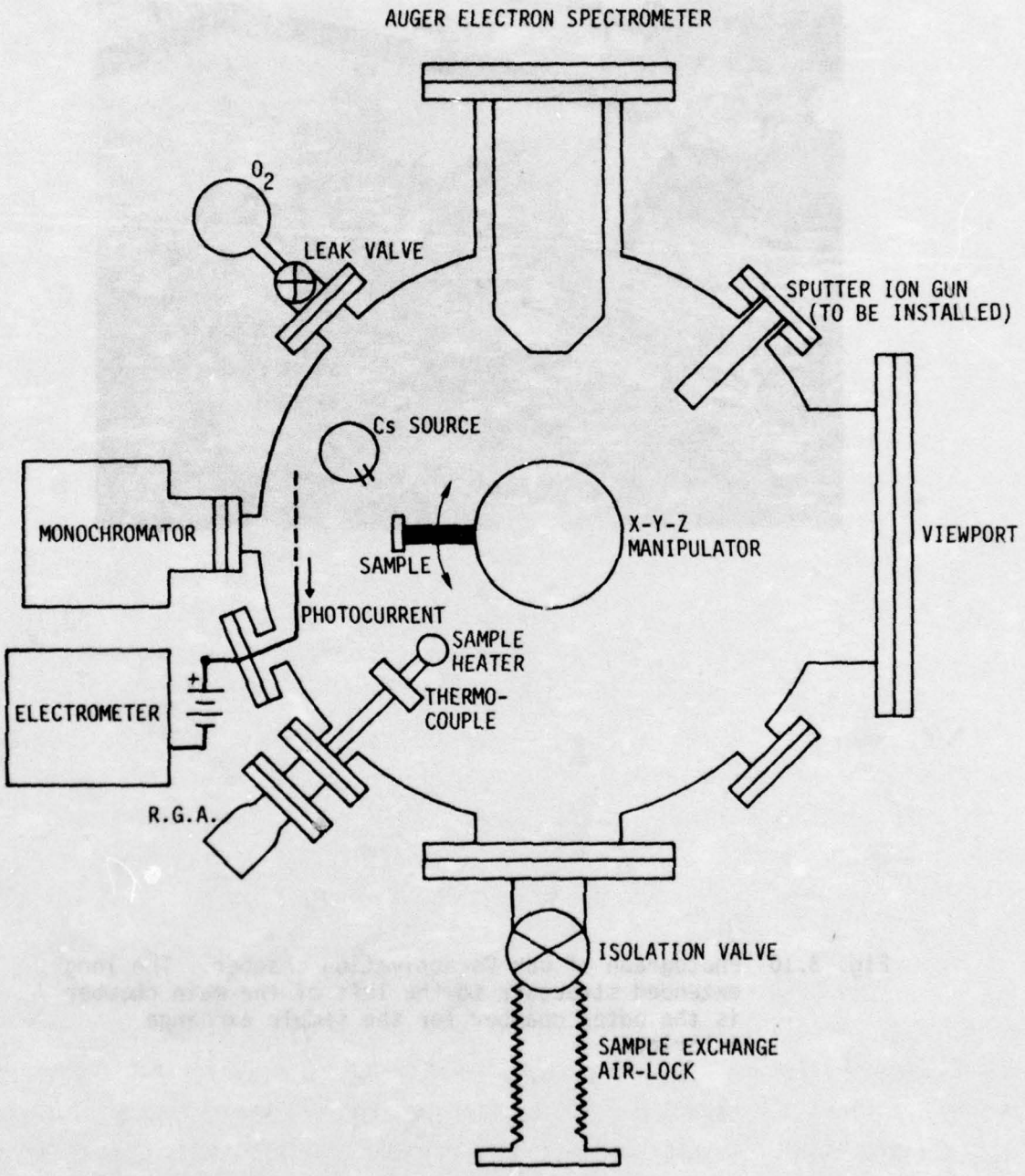



Fig. 3.15 Schematic diagram of photocathode Cs activation system showing relative location of various analytical facilities.

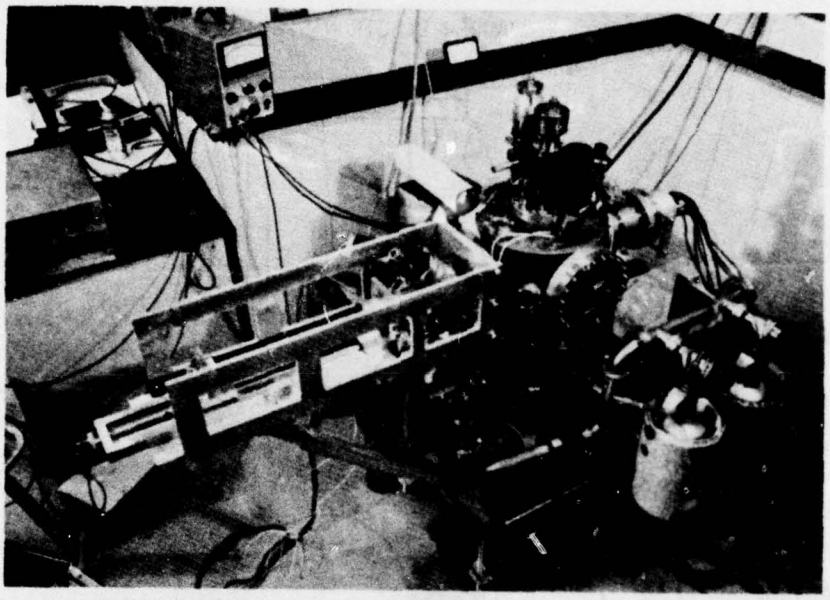


Fig. 3.16 Photograph of our Cs activation chamber. The long extended structure to the left of the main chamber is the outer chamber for the sample exchange interlock.

chamber to air. The large extension and long bellows to the left side of the chamber in Fig. 3.16 constitute the outer sample loading chamber. During the few moments of actual sample transfer between the loading and main chambers, the main chamber pressure rises to the $10^{-10}$ Torr range, however, the pressure returns to the mid $10^{-11}$ Torr range within 2-3 min after resealing the interlock valve. Once in place on the X-Y-Z manipulator (see Fig. 3.15), a sample can be rotated to face the appropriate instrumentation in the chamber which is devoted to various steps in the activation process: surface chemical analysis; surface cleaning; cesium deposition; and photoyield measurement.

Since the Cs activation is a surface chemical reaction, a means for surface chemical analysis of samples is essential for any attempt at optimizing or understanding the relationship between surface processing treatments and photoyield results. For such analysis we rely mainly on Auger electron spectroscopy (AES). AES detects all elements in the periodic table (except H and He) present in the first few atomic layers at a surface with high sensitivity (0.1-0.01 monolayer concentration). Our AES instrumentation permits a real-time display of the surface chemistry with a spatial resolution of $\sim$ 1 mm. This enables us to perform a moderate evaluation of spatial surface variations in elemental concentrations. Also on the chamber is a residual gas analyzer (RGA) with a line of sight view of the sample in the heat cleaning position. This permits analysis of desorbing molecular species from the sample surface during cleaning as well as general analysis of chamber background gases.

It is well known that a necessary condition for obtaining reasonably good photoemissive yields from GaAs is the preparation of an atomically clean sample surface prior to deposition of the initial Cs overlayer. The necessity to activate active semiconductor devices naturally precludes the use of cleaving under vacuum as a method of obtaining clean samples. Semiconductor surfaces exposed to air prior to loading into a vacuum chamber inevitably collect a layer of superficial contamination (for example, CO, $CO_2$, assorted hydrocarbons) and a layer of native oxide that must be removed after the semiconductor sample is in the activation system. The sample surface cleaning under vacuum is done by radiative heating from a quartz-envelope tungsten-halogen lamp.

Heating to ~ 610°C is a standard technique to remove oxides from GaAs.[9] Sample temperature during heat cleaning is monitored by a thermocouple attached to a dummy sample mounted in an identical position behind the heat lamp symmetric to the position of the actual sample which is positioned in front of the lamp. In addition to heat cleaning the surface, we have provision for the installation of an ion gun for sputtering with noble gas ions.

After heat cleaning, the details of which are described in the next section, the sample is positioned to face a monochromator-light source, which is focused to ~ 0.5mm spot on the sample surface. With the monochromator set to pass specular white light from the lamp, a low flux of Cs is directed at the sample. The Cs source is controlled by an UHV valve, which gives close regulation of Cs exposure. A positively biased screen near the sample collects photoelectron current for measurement with an electrometer. Cesium oxide layers are formed by exposing the Cs covered sample to small amounts of high purity bottled $O_2$ leaked into the chamber through a precision valve. Repeated Cs and $O_2$ exposures are made until the white light photoemission is maximized, after which the monochromator is swept through the 0.5-1.0μm wavelength region to obtain spectral photoyield data.

### 3.4.2 Pre-Activation Surface Preparation Studies

As a prelude to actual activation experiments, we initiated a series of experiments to study the effects of various chemical treatments on the surface chemistry of GaAs. After a particular treatment, a surface chemical analysis was obtained using either X-ray photoemission spectroscopy (XPS, also known as ESCA) or an AES analytical system equipped with a sputter ion gun. Both XPS and AES are similar in their sensitivity and the surface depth sampled although XPS is more quantative. These experiments enabled us to find a simple cleaning procedure suitable for initial GaAs activations. Figs. 3.17 and 3.18 shows XPS spectra from GaAs samples which were lightly etched in HF to remove any oxide and then rinsed in methanol (3.17) or water (3.18). The samples were dried in a stream of dry, filtered $N_2$ and transferred in air to the XPS instrument. Measurement of relative peak heights gave the following elemental analysis for the two treated surfaces:

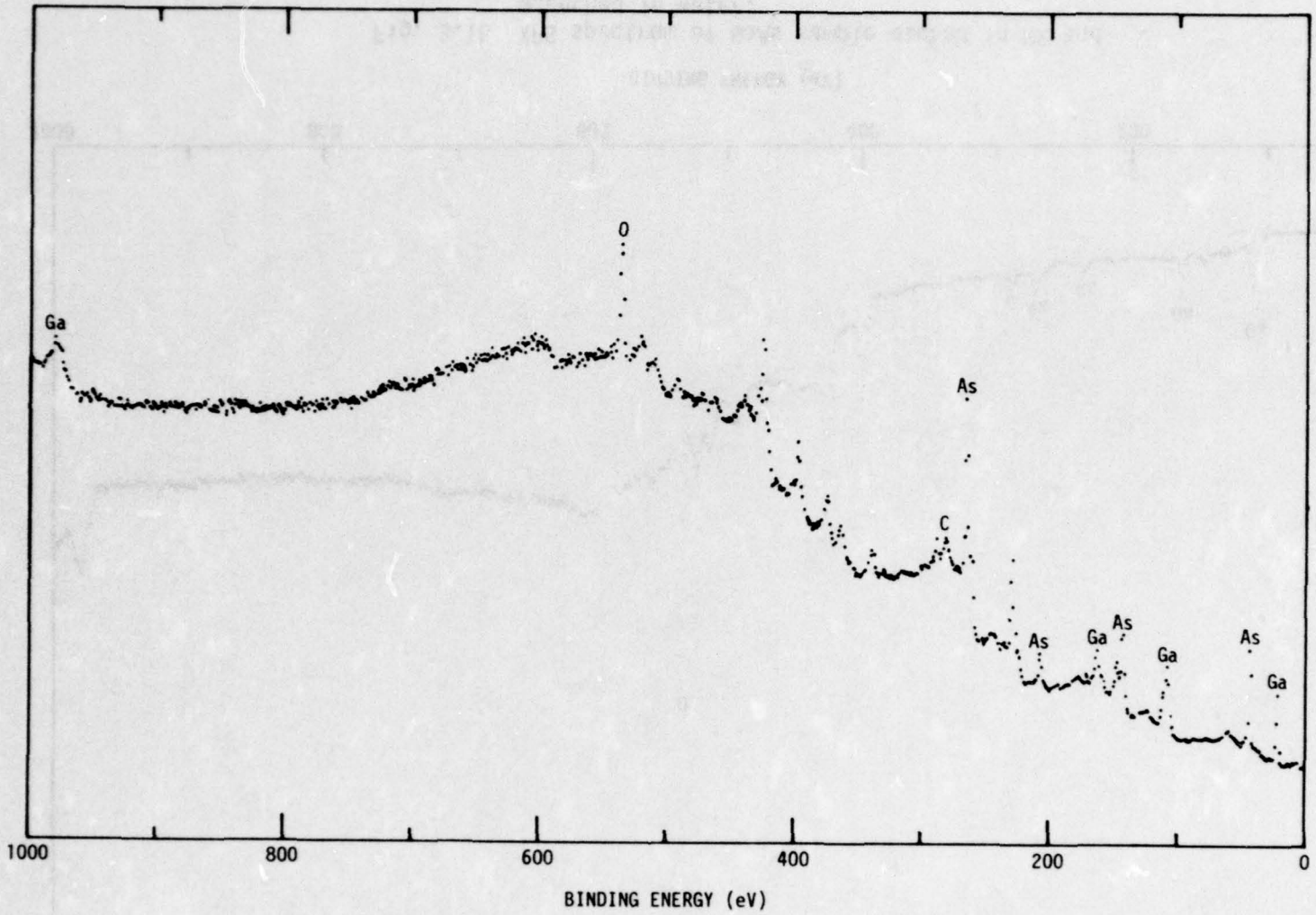



Fig. 3.17 XPS spectrum of GaAs sample etched in HF and quenched in methanol.

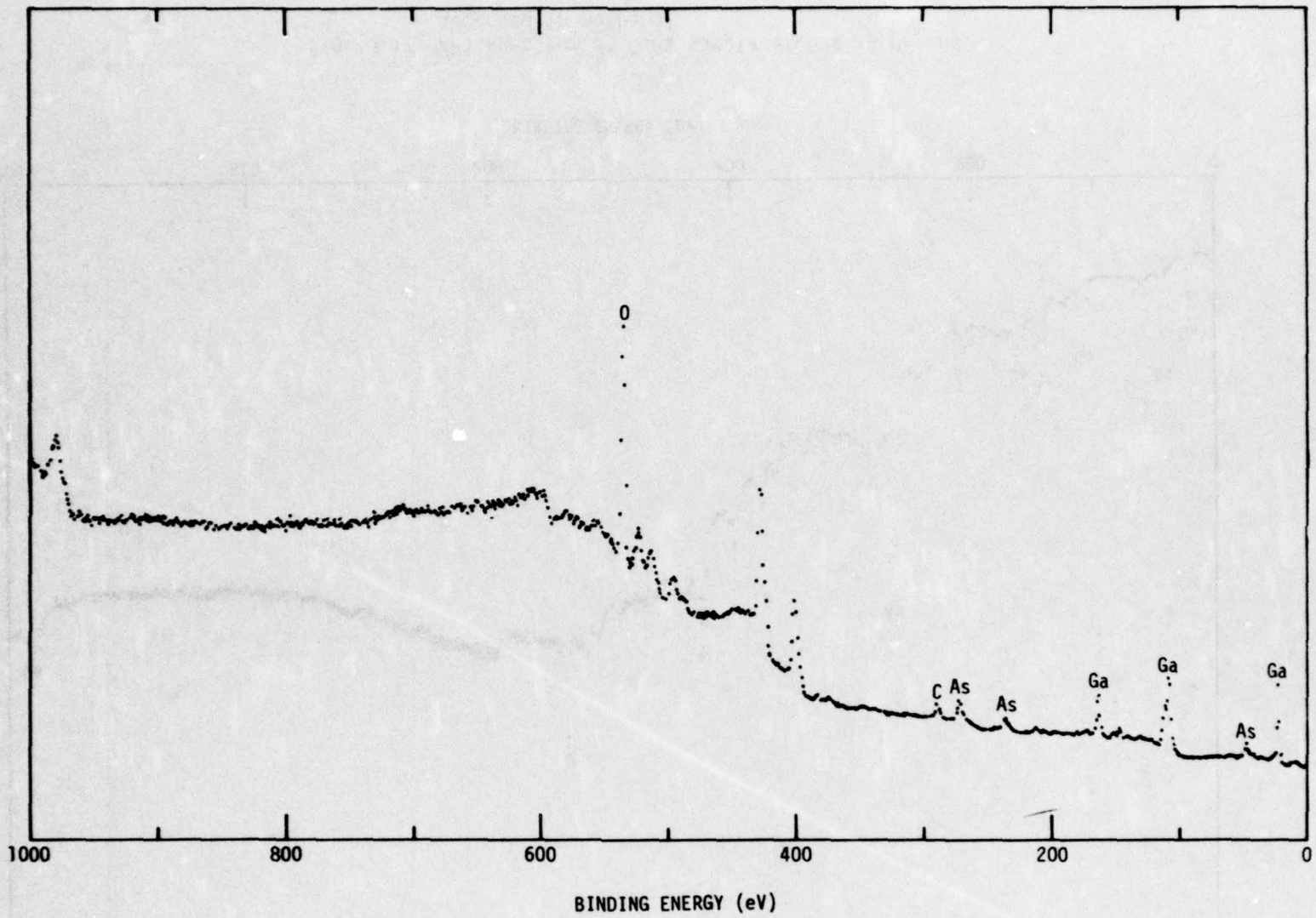



Fig. 3.18 XPS spectrum of GaAs sample etched in HF and quenched in water.

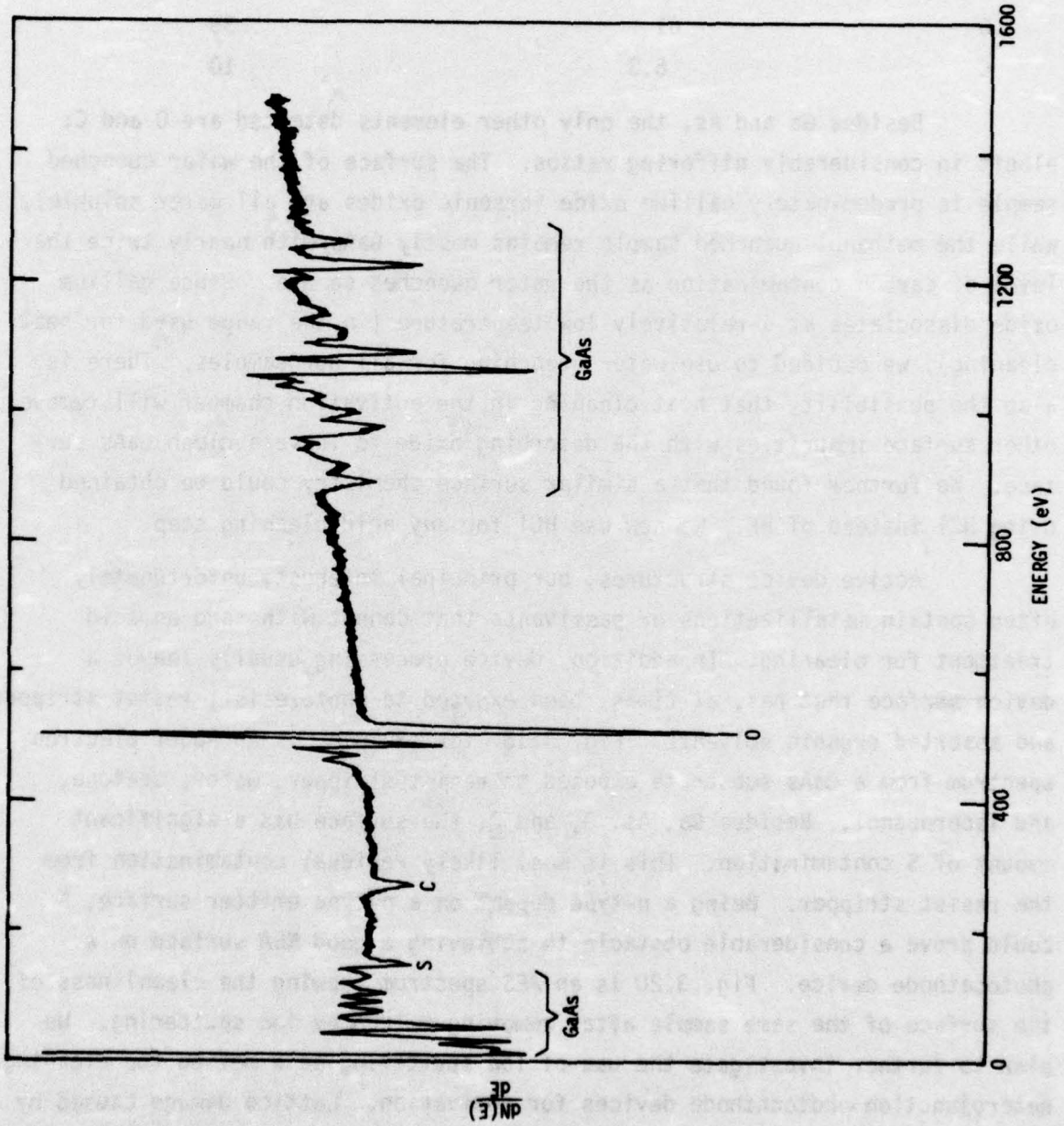



Fig. 3.19 Auger electron spectrum of GaAs sample treated with organic solvents, acid etch, and water quench.

| Element | % of Element (Water Rinse) | % of Element (Methanol Rinse) |
|---|---|---|
| Ga | 30 | 24 |
| As | 2.5 | 27 |
| O | 61 | 38 |
| C | 6.3 | 10 |

Besides Ga and As, the only other elements detected are O and C; albeit in considerably differing ratios. The surface of the water quenched sample is predominately gallium oxide (arsenic oxides are all water soluble), while the methanol quenched sample remains mostly GaAs with nearly twice the level of carbon contamination as the water quenched sample. Since gallium oxide dissociates at a relatively low temperature (in the range used for heat cleaning), we decided to use water quenching for all our samples. There is also the possibility that heat cleaning in the activation chamber will remove other surface impurities with the desorbing oxide to leave a clean GaAs surface. We further found that a similar surface chemistry could be obtained using HCl instead of HF. We now use HCl for any acid cleaning step.

Active device structures, our principal interest, unfortunately often contain metallizations or passivants that cannot withstand an acid treatment for cleaning. In addition, device processing usually leaves a device surface that has, at times, been exposed to photoresist, resist stripper, and assorted organic solvents. Fig. 3.18, for example, is an Auger electron spectrum from a GaAs substrate exposed to resist-stripper, water, acetone, and isopropanol. Besides Ga, As, O, and C, the surface has a significant amount of S contamination. This is most likely residual contamination from the resist stripper. Being a *n*-type dopant on a *p*-type emitter surface, S could prove a considerable obstacle to achieving a good NEA surface on a photocathode device. Fig. 3.20 is an AES spectrum showing the cleanliness of the surface of the same sample after removing ~ 100Å by ion sputtering. We plan to further investigate the use of ion sputtering as a method for cleaning heterojunction photocathode devices for activation. Lattice damage caused by the sputtering is a potential problem when using ion bombardment for cleaning. However, the present studies on surfaces which have been treated with organic

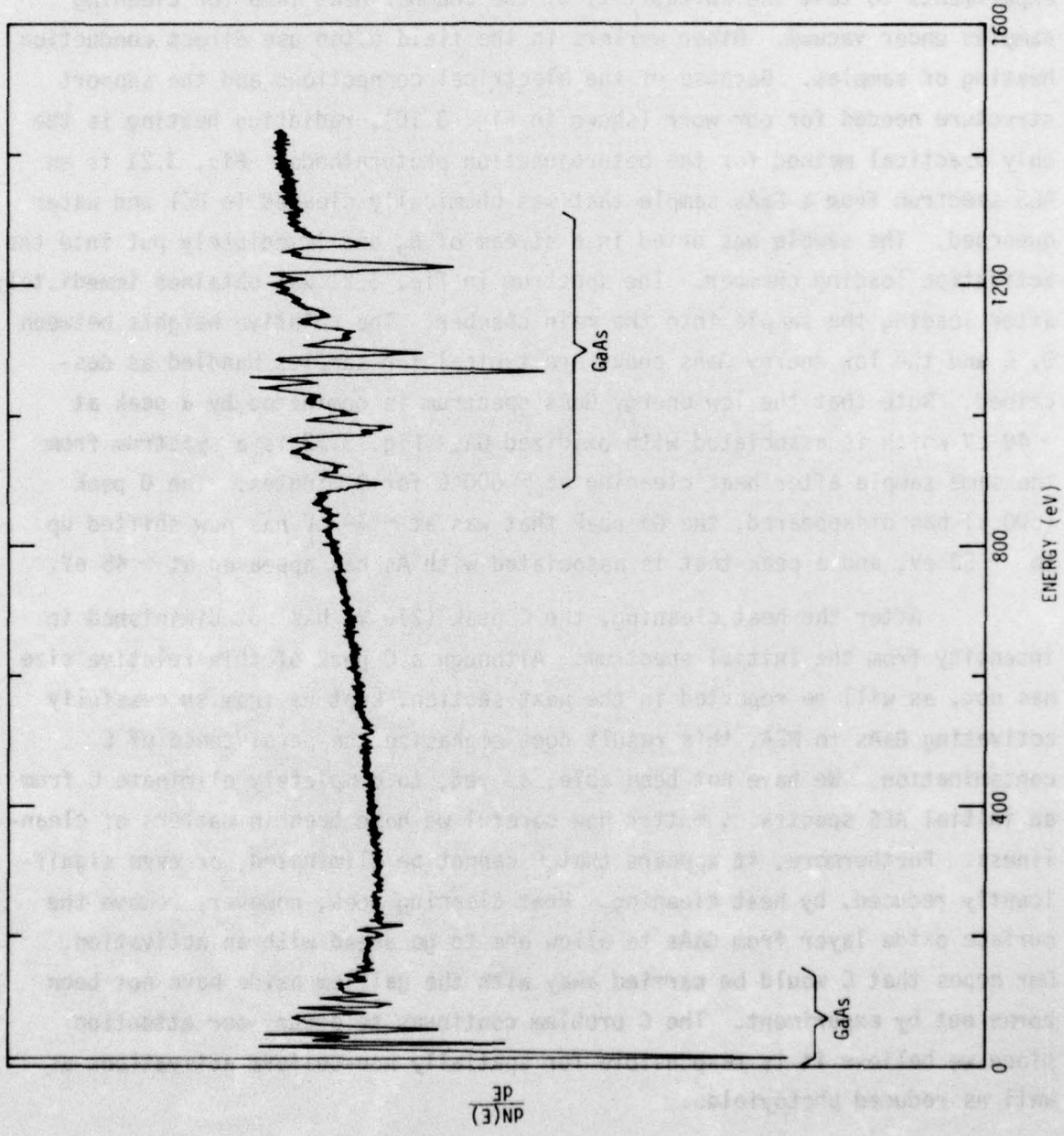



Fig. 3.20 Same sample as Fig. 3.19 after 100Å of surface removal by ion sputtering.

cleaners indicate that sputter cleaning may be the only way to obtain a truly clean surface.

Upon completion of the activation chamber, we immediately began experiments to test the suitability of the chamber heat lamp for cleaning samples under vacuum. Other workers in the field often use direct conduction heating of samples. Because of the electrical connections and the support structure needed for our work (shown in Fig. 3.10), radiation heating is the only practical method for the heterojunction photocathode. Fig. 3.21 is an AES spectrum from a GaAs sample that was chemically cleaned in HCl and water quenched. The sample was dried in a stream of $N_2$ and immediately put into the activation loading chamber. The spectrum in Fig. 3.21 was obtained immediately after loading the sample into the main chamber. The relative heights between O, C and the low energy GaAs peaks are typical for samples handled as described. Note that the low energy GaAs spectrum is dominated by a peak at ~ 49 eV which is associated with oxidized Ga. Fig. 3.22 is a spectrum from the same sample after heat cleaning at ~ 600°C for 3 minutes. The O peak (500 V) has disappeared, the Ga peak that was at ~ 49 eV has now shifted up to ~ 53 eV, and a peak that is associated with As has appeared at ~ 45 eV.

After the heat cleaning, the C peak (270 V) has not diminished in intensity from the initial spectrum. Although a C peak of this relative size has not, as will be reported in the next section, kept us from successfully activating GaAs to NEA, this result does emphasize the persistence of C contamination. We have not been able, as yet, to completely eliminate C from an initial AES spectra no matter how careful we have been in matters of cleanliness. Furthermore, it appears that C cannot be eliminated, or even significantly reduced, by heat cleaning. Heat cleaning does, however, remove the surface oxide layer from GaAs to allow one to go ahead with an activation. Our hopes that C would be carried away with the gallium oxide have not been borne out by experiment. The C problem continues to occupy our attention since we believe it is responsible for spatially non-uniform activations as well as reduced photoyields.

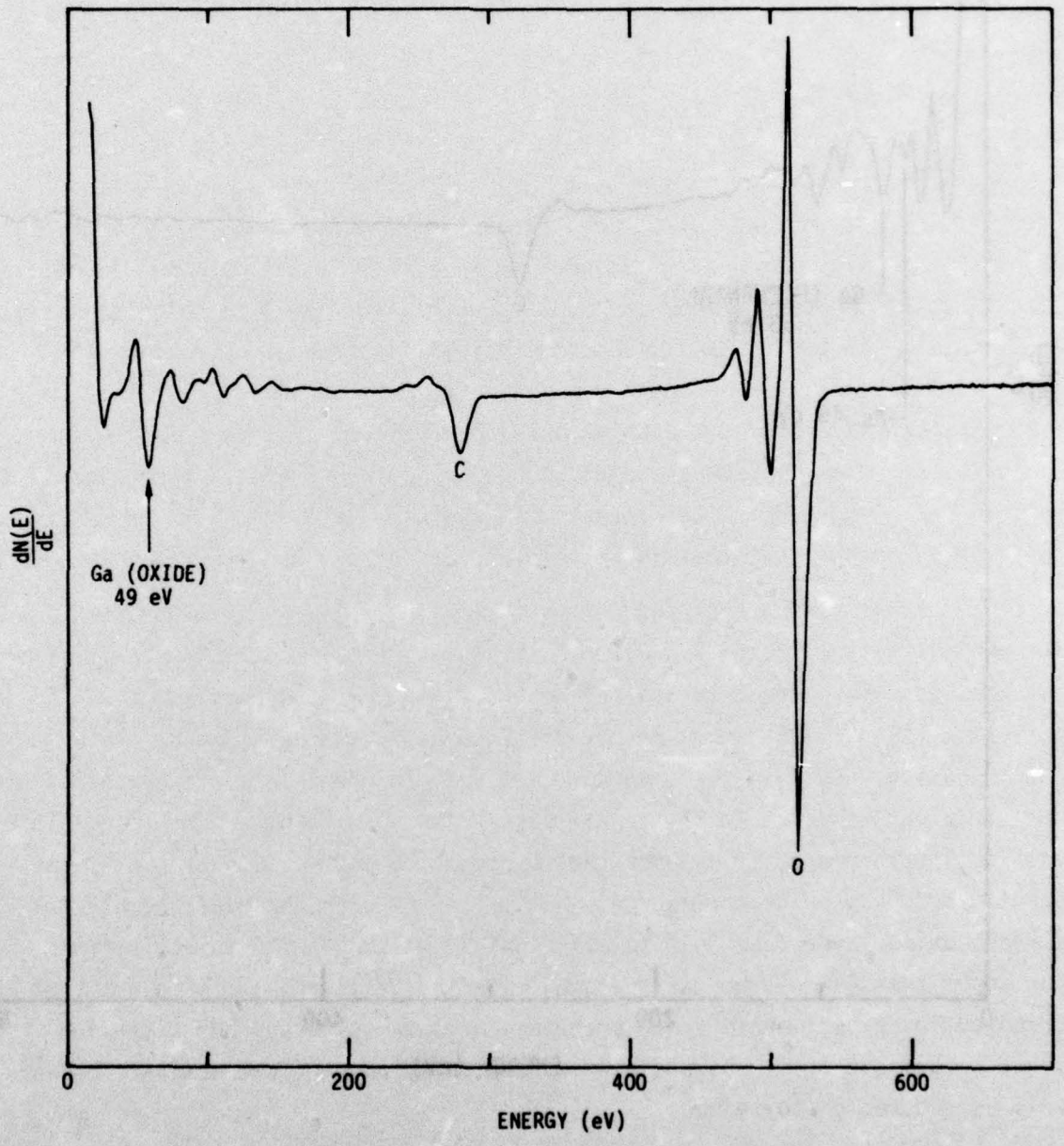



Fig. 3.21 Auger electron spectrum of GaAs sample before heat cleaning.

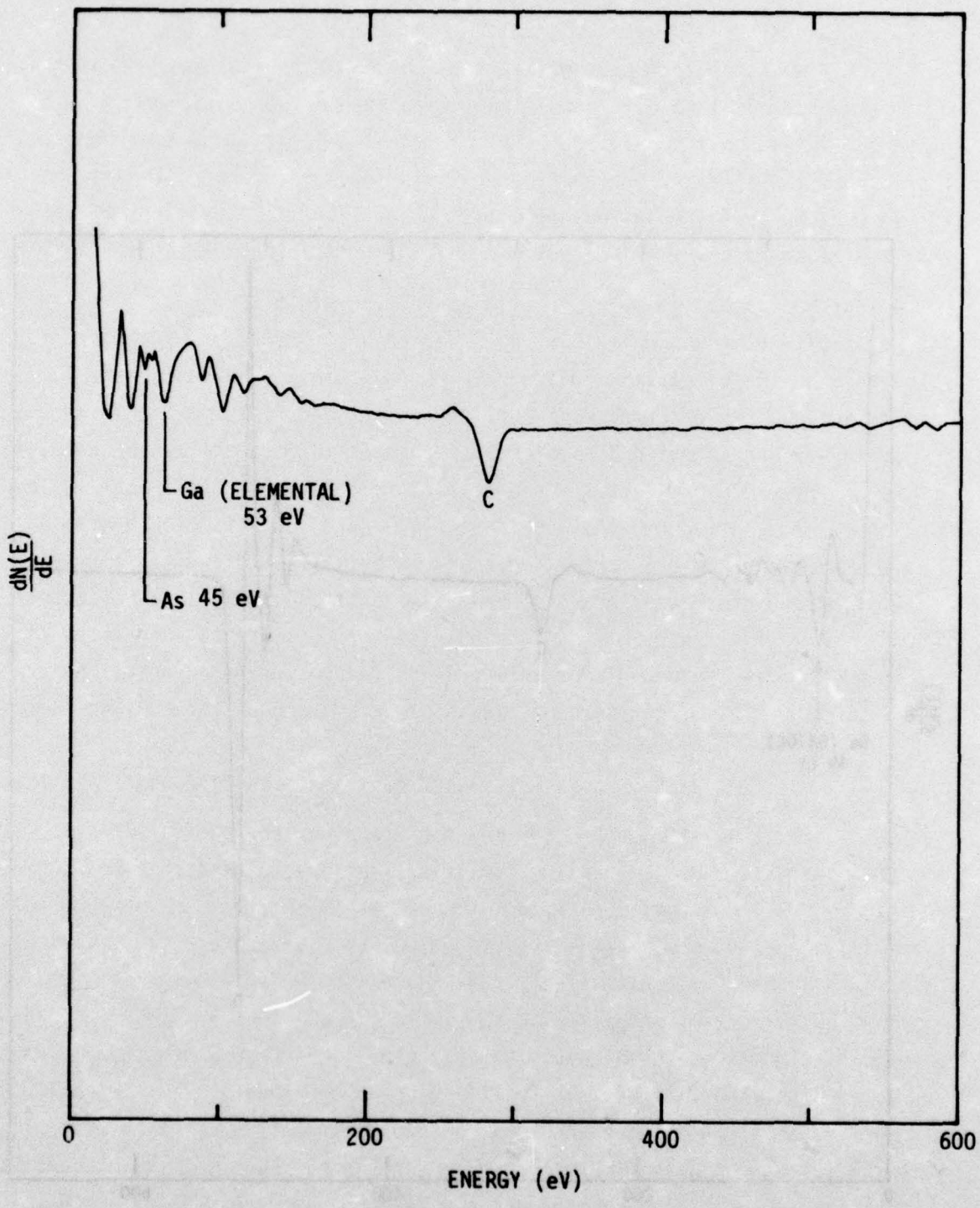



Fig. 3.22 Spectrum yield curve of GaAs epitaxially grown layer after activation to NEA.

### 3.4.3 Cs Activation Results

Once a sample has been cleaned under vacuum activation can proceed. Activation proceeds by first depositing Cs onto the sample until a peak in white light sensitivity is reached. Then $O_2$ is admitted into the chamber until a second, higher photoemission peak is observed. Alternate Cs and $O_2$ applications are continued until two successive $Cs/O_2$ cycles result in the same value of peak white light photoemission. Photoemissive yield versus wavelength measurements are then made to characterize the activation.

After an initial experiment with $p^+$-Zn doped GaAs substrate material, we began activating $p^+$-Ge doped epitaxial GaAs layers that are identical to the emitter layer of the photocathode device. In this way we could develop our activation procedures to optimize the photoemissive yields on our photocathode emitter surfaces. A yield curve showing the spectral response versus wavelength, $\lambda$, between 0.5 and 1$\mu$m from one of our activated epitaxial layers is shown in Fig. 3.23. Fig. 3.24 is the data in Fig. 3.23 replotted as $\frac{1 - R(\lambda)}{Y(\lambda)}$ vs. $\frac{1}{\alpha(\lambda)}$, where Y is the yield in electrons per incident photon, R is the GaAs reflection coefficient, and $\alpha$ is the GaAs absorption coefficient, each as a function of wavelength.

Using a diffusion model for photoemitted electrons,[10] the yield at long wavelengths can be expressed as:

$$\frac{1 - R(\lambda)}{Y(\lambda)} = \frac{1}{p}\left(1 + \frac{1}{\alpha(\lambda) L}\right)$$

where p is the escape probability for thermalized electrons at the GaAs-$Cs_2O$ interface and L is the electron diffusion length. Using the above equation, we obtain a value of p from the intercept of a line drawn through the points corresponding to $.76 \leq \lambda \leq .86$ and a value for L from the slope of this line. The line drawn represents photoemission resulting from thermal electrons populating the $\Gamma$ - conduction band minimum, while the departure from this line at shorter wavelengths indicates a contribution from both hot photoelectrons in $\Gamma$ and thermal electrons populating the higher X-conduction band

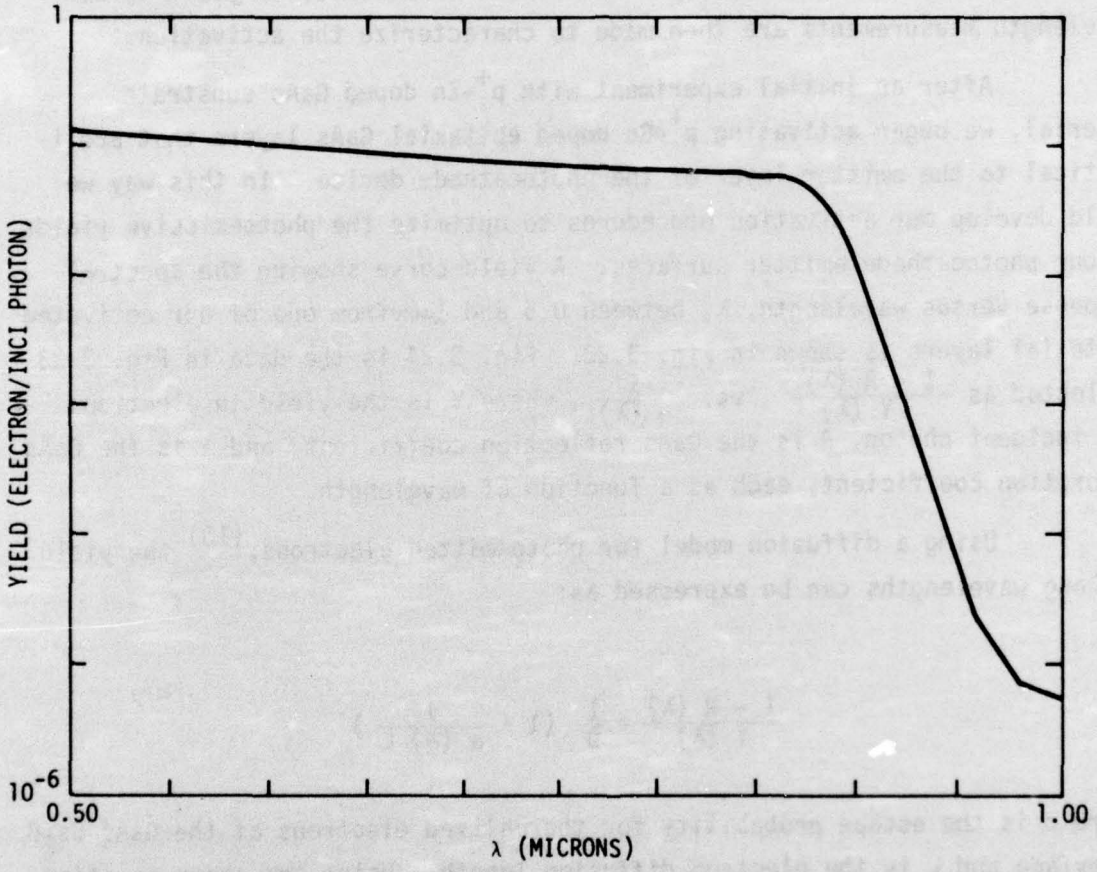



Fig. 3.23 Spectrum yield curve of GaAs epitaxially grown layer after activation to NEA.

minima. The above elementary model is appropriate only at longer wavelengths near photoemission threshold where all of the photoelectrons are thermalized in Γ.

From Fig. 3.24 we obtain p = 11% and L = 5.2μm. Analyzing the yield data from a plot like Fig. 3.24 provides far more insight into the material and activation quality than a spectral yield curve alone. As can be seen from Fig. 3.23, the yield at 0.5μm is above 10%. The overall yield for this layer is 453μm Amps/lumen, a reasonable number considering that there is the degree of C contamination shown in Fig. 3.22. While we hope to continually improve our activation technique, an activation of this quality on a finished photocathode device is certainly sufficient to test the device operation. Once the C contamination problem is under better control the quality of the activations will improve accordingly.

In addition to the activation work at the Science Center, some preliminary work on activating heterojunction devices was carried out by Dr. John Pollard at the U.S. Army Night Vision Laboratories. Because of the complex nature of the double heterojunction photocathode, we decided that many of our questions regarding active device activation could be answered by studying a GaAlAs-GaAs heterojunction "cold cathode." Some earlier work had been done on GaAs cold cathodes[11] but these devices did not have an ohmic contact to the emitter, only a W probe to the surface. Although a probe contact is very poor from the standpoint of current crowding and device performance, it does circumvent the problems created by heating ohmic contacts to the GaAs heat cleaning temperature.

Our cold cathode device is shown schematically in Fig. 3.25. Note that it is identical to the hole barrier (HB) and emitter (E) portions of the field assisted photocathode (Figs. 1.1 and 2.6). In the cold cathode, the E-HB junction is forward biased so that electrons are injected from the n-GaAlAs layer into the $p^+$-GaAs emitter. These electrons diffuse through the emitter to the NEA surface and are emitted into vacuum. These cold cathode structures are used to study the effects of heat cleaning, sputtering, and Cs activation on the electron transport properties of the emitter layer, degradation of the E-HB junction, and any undesireable effects from the ohmic contacts

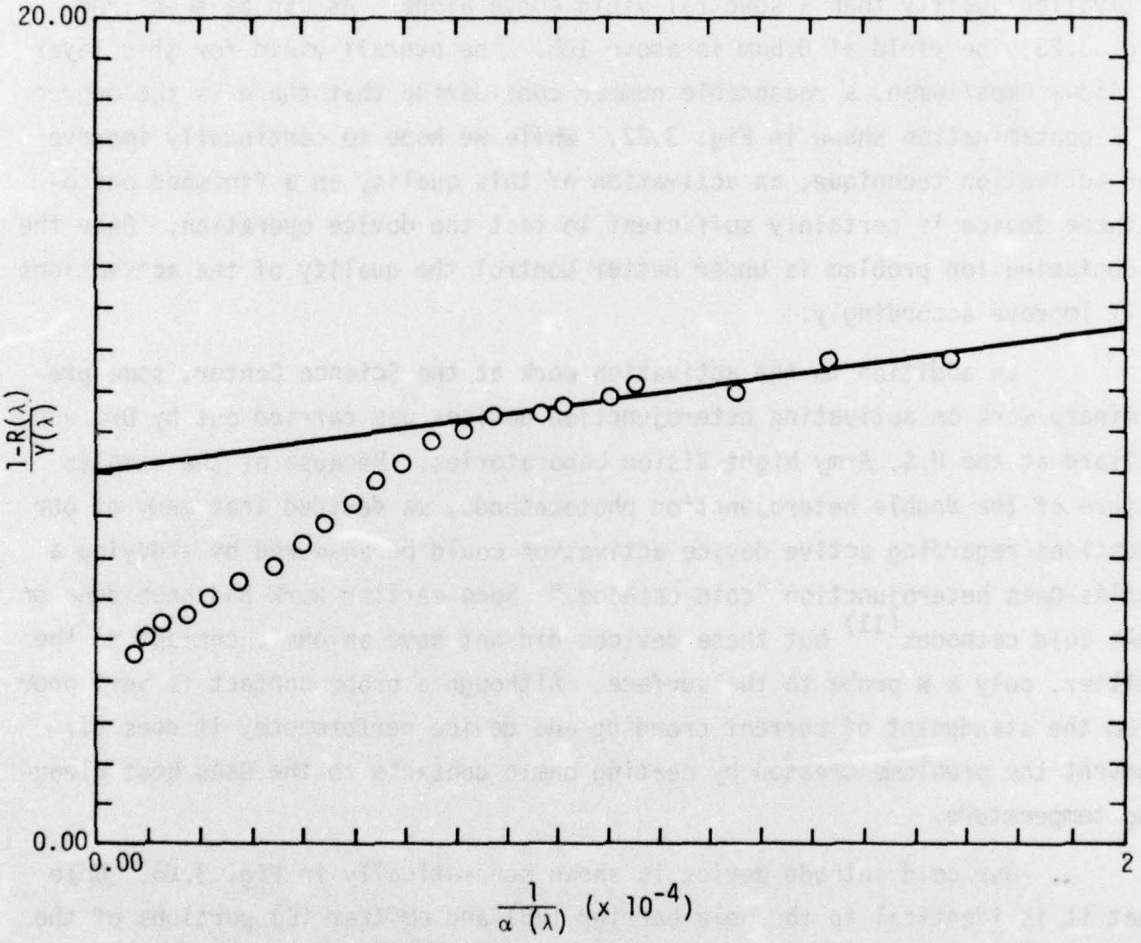



Fig. 3.24 Plot of 1-R/Y vs. 1/α for yield curve of Fig. 3.23.

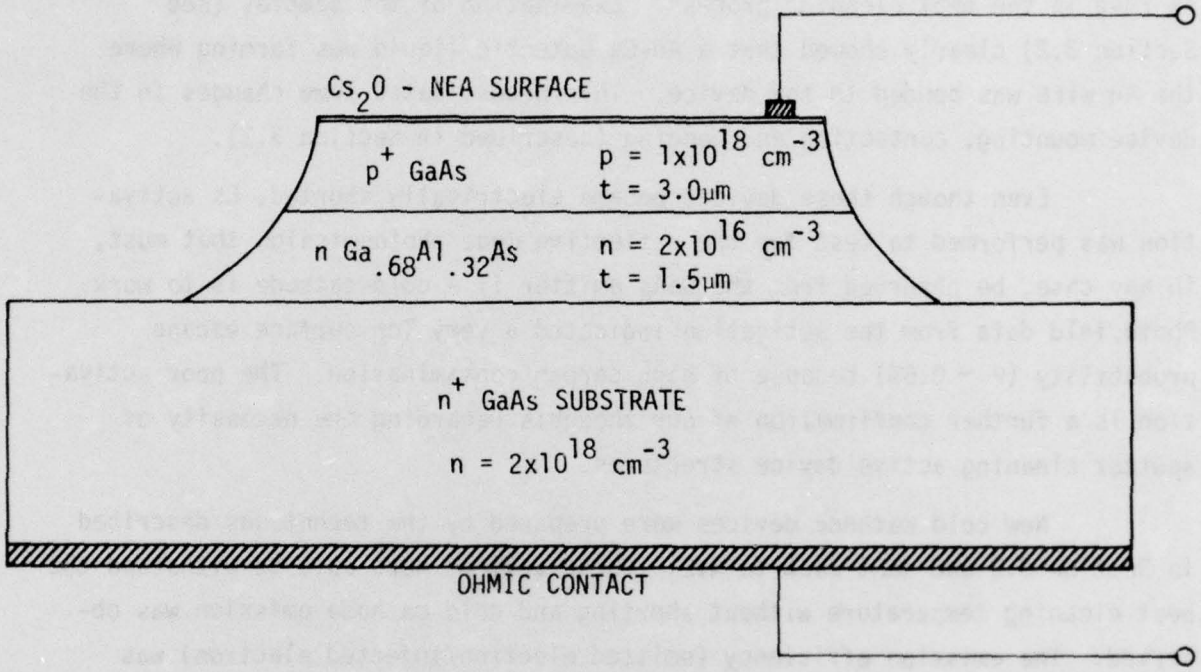



Fig. 3.25 Schematic view of GaAs-GaAlAs heterojunction cold-cathode structure.

or mesa surfaces.

The first set of devices sent to Dr. Pollard were, in turn, (a) placed in his chamber, (b) the I-V characteristic measured, (c) heat cleaned at 625°C for several minutes, (d) allowed to cool to room temperature and, (e) the I-V characteristic was remeasured. Every one of the devices became shorted in the heat cleaning process. Examination of the samples (see Section 3.2) clearly showed that a Au-Ga eutectic liquid was forming where the Au wire was bonded to the device. This necessitated some changes in the device mounting, contacting and bonding (described in Section 3.2).

Even though these devices became electrically shorted, Cs activation was performed to test for the reflective mode photoemission that must, in any case, be observed from the GaAs emitter if a cold-cathode is to work. Photoyield data from the activation indicated a very low surface escape probability ($P \sim 0.5\%$) because of high carbon contamination. The poor activation is a further confirmation of our thoughts regarding the necessity of sputter cleaning active device structures.

New cold cathode devices were prepared by the techniques described in Section 3.2 and sent back to NVL. These devices were able to withstand the heat cleaning temperature without shorting and cold cathode emission was observed. The emission efficiency (emitted electron/injected electron) was still very low, $\sim .002\%$, because of the carbon problem and also, after Cs activation, the mesa surfaces contributed a very high leakage current. The above efficiency is calculated assuming the total bias current is contributing injected electrons. Of the total forward current, however, the high surface leakage current may well be 10 or 100 times greater than the actual injected electron current. Thus, the above efficiency value cannot be directly compared to expected photocathode performance. These measurements do show, however, that the ohmic contact problems have been solved and that a heterojunction structure can withstand heat cleaning and activation processing. These results confirm that procedures for sputter cleaning and mesa surface protection must be developed to achieve a satisfactory device.

At about the time the newer cold cathode structures were activated

at NVL, our Science Center activation capability became established (results of our first activations on GaAs were described earlier). At this point, we had two of the etch-thinned photocathode structures available so we decided to try to activate these devices rather than pursue improvement of the cold cathode activation. Because of the fragile nature of the photocathode devices (thinned to ~ 20μm) and their mounting on a ceramic holder, they had to be heated by radiation rather than conduction. Since our chamber was built for radiative heating and the NVL chamber would require considerable modification to do so, all of the thinned structures will be activated at the Science Center.

The samples were prepared as outlined in Section 3.2. These devices have an etch-thinned active region that is ~ 2mm square and ~ 20μm thick. The yield in preparing these samples is very poor because the thin unsupported active device area breaks very easily. By perseverance, two of these samples were successfully mounted and prepared for activation. Both of these samples suffered the same fate; they broke during heat cleaning under vacuum in the activation chamber. The problems encountered with this particular structure render a virtually hopeless situation because the device is so fragile. The lattice mismatch between the GaAsSb absorber and the remaining GaAs and GaAlAs layers creates considerable mechanical strain within the device even without heating. Even more damaging, however, are the thermal stresses created during heating. Because the device is so thin, non-uniform heating occurs and there is a very large thermal gradient at the active device edge where the sample becomes much thicker. These problems must be eliminated in order to activate a heterojunction photocathode.

A new type of device structure is required in which the entire device, while thin, is structurally supported by some other material. This structural support must have a good thermal expansion match to the photocathode structure and have good thermal conductivity so as to reduce the non-uniform heating. Such an improved device structure is described in the following section.

## 4.0 CONCLUSIONS AND RECOMMENDATIONS

During the course of this program, major emphasis has been on developing a Cs activation technology and heterojunction photocathode processing which is compatible with the activation requirements. We successfully built an activation chamber and demonstrated photoemission into vacuum from a GaAs-NEA photocathode. An etch thinning technique has been developed for removing the GaAs substrate to expose the emitter surface of the device. A new ohmic contact utilizing tungsten with Ag-Mn has proven successful in withstanding the high heat cleaning temperature (~ 610°C). Cold cathode devices were successfully activated and emission into vacuum was observed from a p-n heterojunction device.

Based on the results of this program, we conclude that the double heterojunction approach is still a promising structure to realize a hign sensitivity 1.06μm photocathode. Nearly all of the necessary device processing and activation techniques have been developed. The physical structure of our present device is now the limiting factor because it will not withstand the thermal stresses created during activation. The solution to this problem is to design and fabricate a device structure in which the thin active device area is structurally supported to eliminate both the breakage and thermal stress problems.

A device structure which should fulfill the above requirements has been designed and it is shown in the schematic diagram of Fig. 4.1. This is the same initial device structure which we used in this program (see Figs. 2.6 and 3.7). The only difference occurs in mounting where the device will now be bonded to a second GaAs substrate with the absorber down rather than substrate down. The substrate removal is now similar to that described in Section 3.2 except that the entire substrate is removed rather than only the selected areas through the holes in the ceramic. This new device is completely supported by the second GaAs substrate which should eliminate the breakage problem.

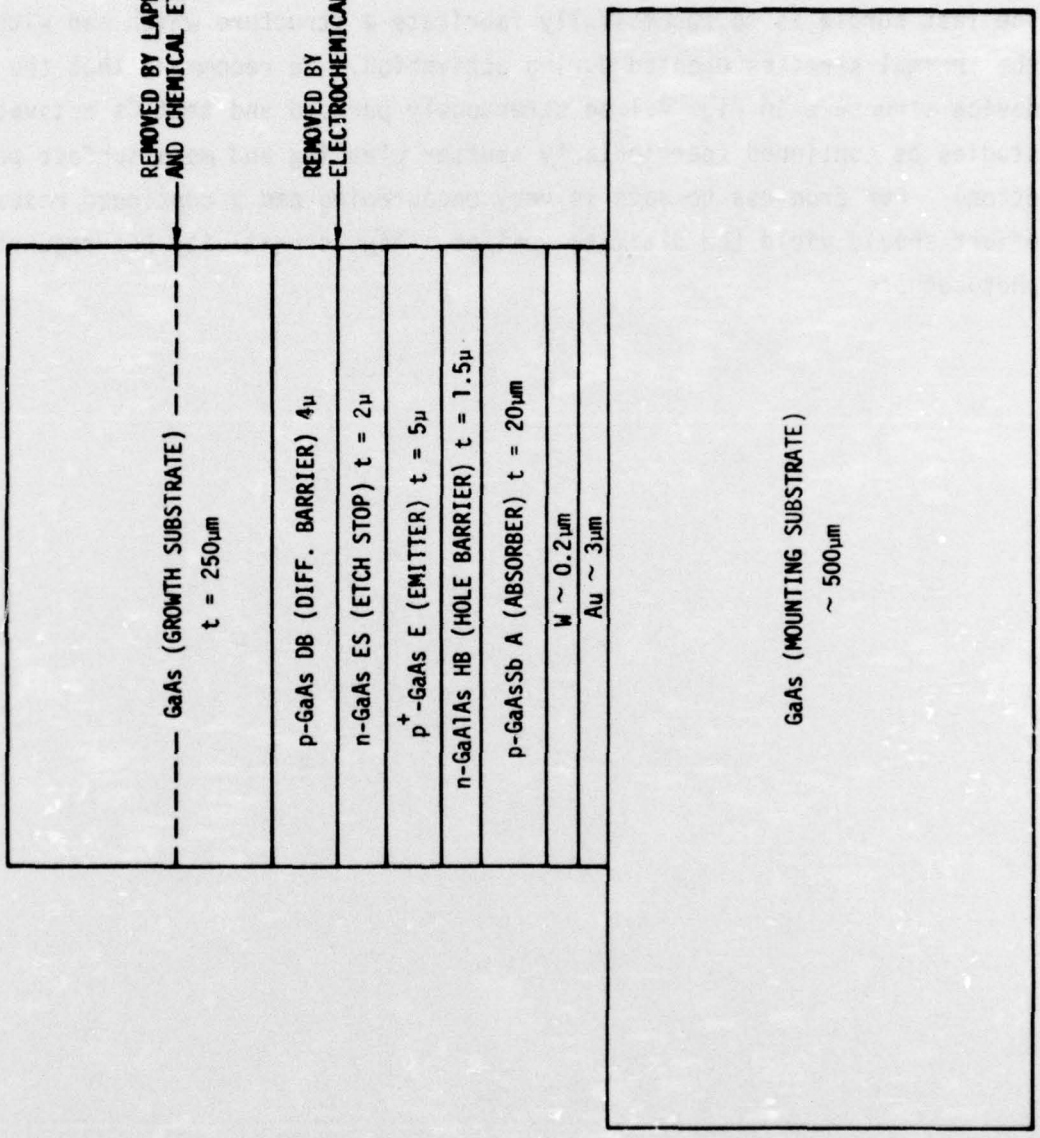



Fig. 4.1 The proposed new device structure in which the epitaxial structure is eutectically honded, absorber down, to a second GaAs substrate. The original GaAs growth substrate is then selectively removed by a combination of lapping and chemical and electrolytic etching to expose the emitter surface.

At this point in the research effort, nearly all of the elements necessary for demonstration of field assisted photoemission have been realized. The last hurdle is to successfully fabricate a structure which can withstand the thermal stresses created during activation. We recommend that the new device structure in Fig. 4.1 be strenuously pursued and that Cs activation studies be continued (particularly sputter cleaning and mesa surface passivation). Our progress to date is very encouraging and a continued research effort should yield the ultimate goal of a high sensitivity heterojunction photocathode.

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